Universal Asynchronous Receiver/Transmitter (UART)

Key Features

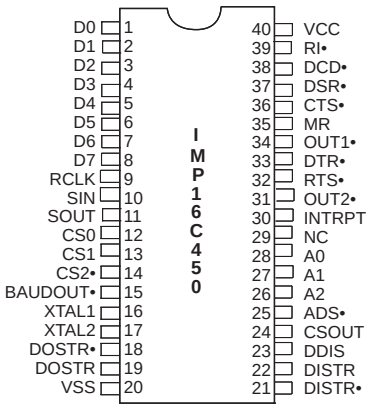
- 5V Operation
- Full duplex asynchronous receiver and transmitter
- Easily interfaces to most popular microprocessors
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from a serial data stream
- Independently controlled transmitter, receiver, line status, and data set interrupts
- Programmable baud rate generator allows division of any input clock by 1 to (2^{16}-1) and generates the internal 16 x clock
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
  - Baud generation (DC to 56k baud)
- False start bit detection
- Complete status reporting capabilities
- Tri-State® TTL drive capabilities for bi-direc tional data bus and control bus
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity overrun, and framing error simulation
- Fully prioritized interrupt systems controls

General Description

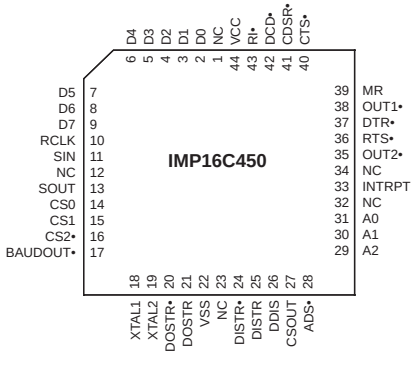
IMP16C450 Universal Asynchronous Receiver Transmitter (UART) is a CMOS-VLSI communication device in a single package.

The UART performs serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversions on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operation being performed by the UART, as well as any error conditions (parity, overrun, framing, or break detect).

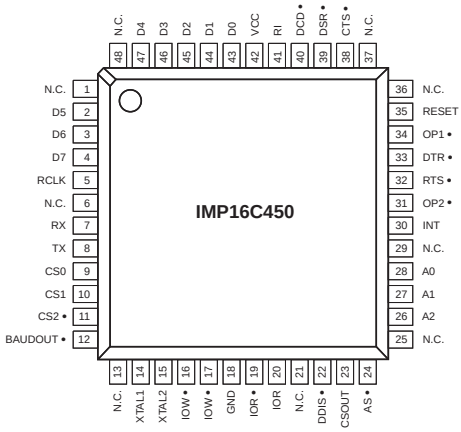
Pin Configuration



40-PIN DIP



44-PIN PLCC



48-PIN TQFP

The IMP16C450 UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that capable of dividing the timing reference clock input by divisor of 1 to (2^{16}-1), and producing a 16 x clock to drive the internal transmitter logic. Provisions are also included to use this 16 x clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor interrupts system. Interrupts can be programmed to the user's the requirements, minimizing the computing required to handle the communications link. UART is designed to work either in a polled or an interrupt driven environment selected by software.

The UART is fabricated using IMP's advanced double metal CMOS process.

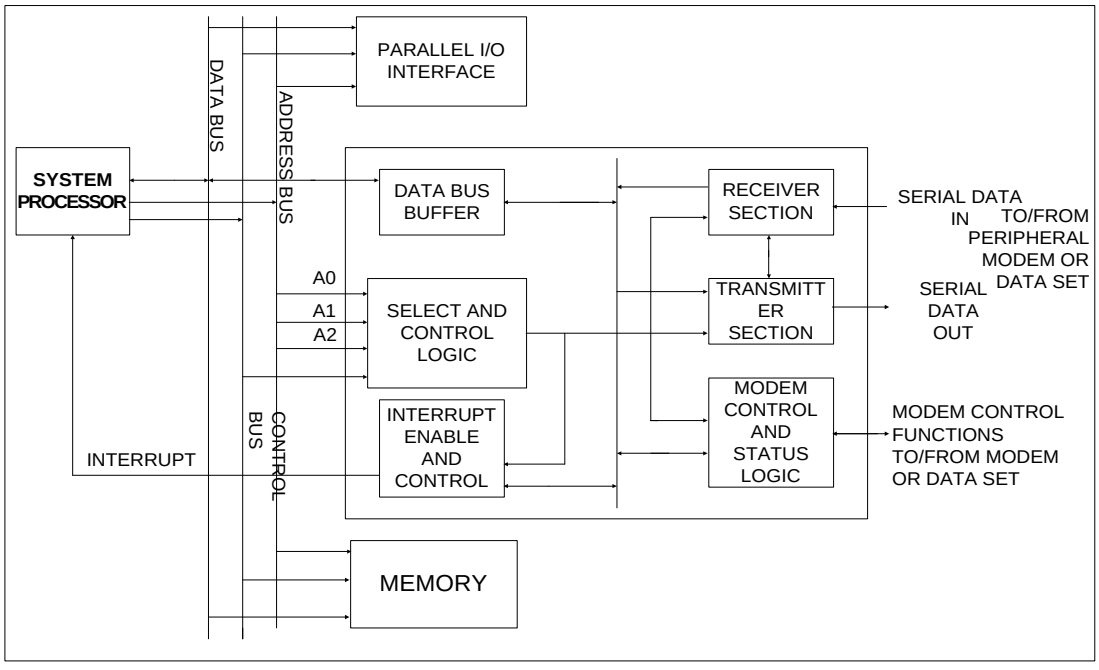


FIGURE 1 – IMP16C450 General System Configuration

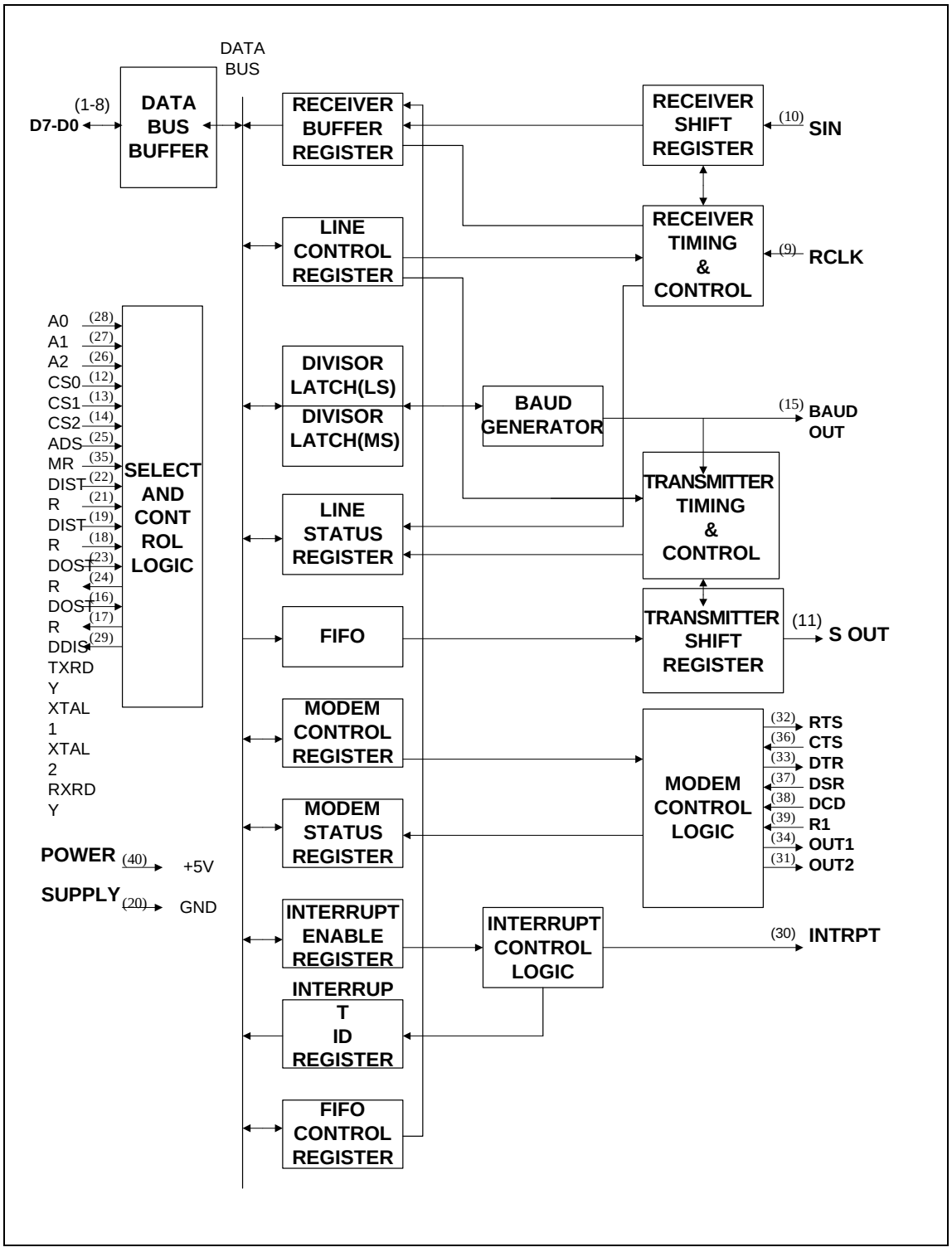


FIGURE 2 – IMP16C450 Block Diagram

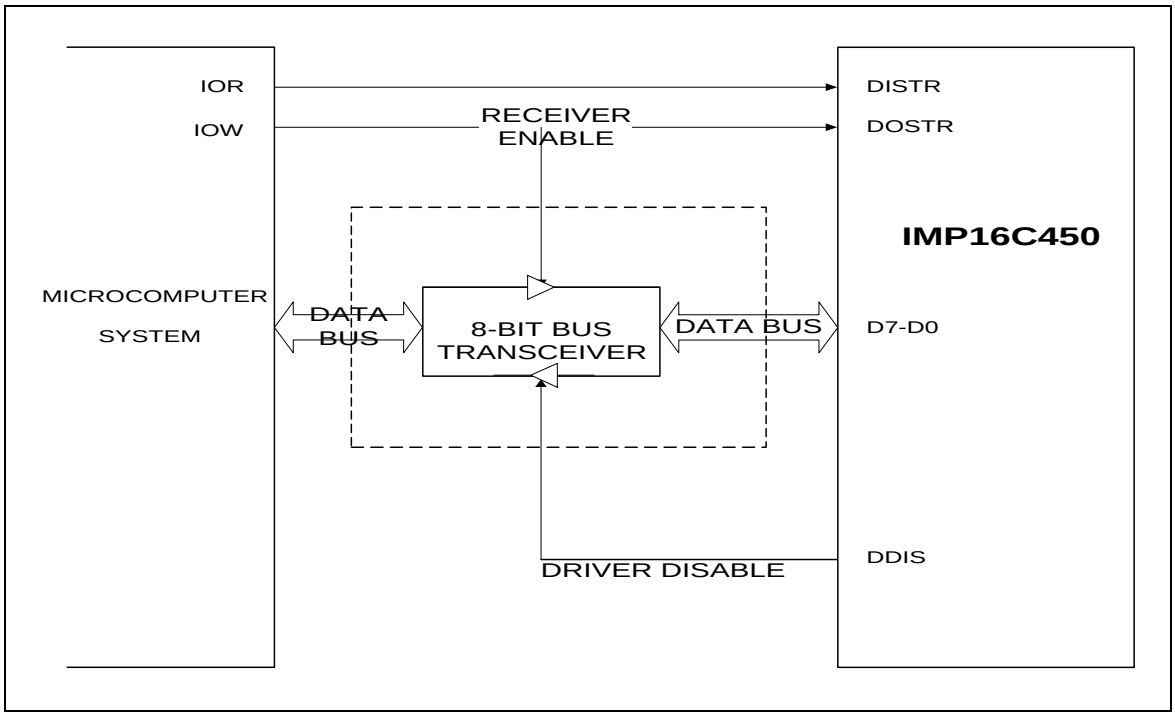


FIGURE 3 – Typical Interface for a high-capacity data bus

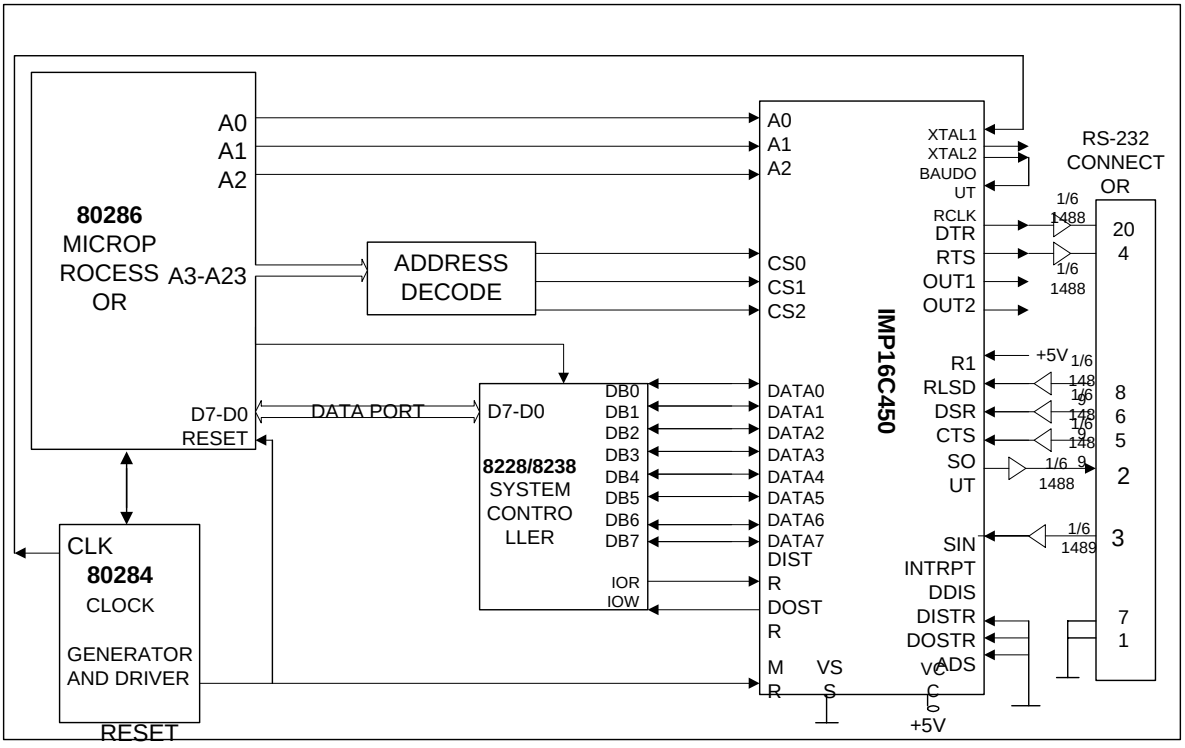


FIGURE 4 – Typical 16-Bit Microprocessor/RS-232 Terminal Interface using the UART

Pin Description

Note: In the following descriptions, a low represents a logic 0 and a high represents a logic 1

Mnemonic	Pin type	PIN # for 40-DIP/ 44-PLCC	Description
CS0,CS1 CS2*	IN	12:14/14:16	Chip select pins: When CS0 and CS1 are high and CS2* is low, the chip is selected. This enables communication between the UART and the CPU. The positive edge of the active address strobe signal latches the decoded chip select signals, completing chip selection. If ADS* is always low, valid chip selects should stabilize according to the CSW parameter.
DISTR* DISTR	IN	23,24/25,26	Data in strobe: When DISTR is high or DISTR* is low while the chip is selected, The CPU can read status information or data from the selected UART register. Note: Only an active DISTR or DISTR* input is required to transfer data from the UART during a read operation. Therefor, tie either DISTR input permanently low or the DISTR* input permanently high, when it is not used.
DOSTR* DOSTR	IN	18,19/20,21	Data out strobe: When DOSTR is high or DOSTR* is low while the chip is selected, the CPU can write control words or data into the selected UART register. Note: Only an active DOSTR or DOSTR* input is required to transfer data to the UART during the write operation. Therefor, tie either DOSTR input permanently low or the DOSTR* input permanently high, when it is not used.
ADS*	IN	25/28	Address strobe: The positive edge of an active address strobe signal (ADS*) latches the Register select pins (A0, A1, A2) and chip selects signals (CS0, CS1, CS2*). Note: An active ADS* input is required when the Register select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the ADS* input permanently low.
A2,A1, A0	IN	26:28/29:31	Register select pins: Address signals connected to these 3 inputs select a UART register for the CPU to read from or write to during data transfer. A table of register and their address is shown below. Note that the state of the Diver Latch Access Bit (DLAB), which is the most significant bit of the line control register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches. REGISTER ADDRESS DLAB A2 A1 A0 Register 0 0 0 0 Receiver Buffer Register (read) 0 0 0 0 Transmitter Holding Register (write) 0 0 0 0 Interrupt Enable Register x 0 1 0 Interrupt Identification Register (read) x 0 1 1 Line Control Register x 1 0 0 MODEM Control Register x 1 0 1 Line Status Register x 1 1 0 MODEM Status Register x 1 1 1 Scratch Pad Register 1 0 0 0 Divisor Latch Register (Least significant byte) 1 0 0 1 Divisor Latch Register (Most significant byte)

Mnemonic	Pin type	PIN # for 40-DIP/ 44-PLCC	Description
MR	IN	35/39	**Master Reset:** When this input is high, it clears all the registers (except the Register Buffer, Transmitter Holding and Divisor Latches), and the control logic of the UART. The states of various output signals (SOUT, INTR, OUT1*, OUT2*, RTS*, DTR*) are affected by an active MR input (Refer to Table 1).this input is buffered with a TTL-compatible Schmitt Trigger with 0.5V typical hysteresis.
RCLK	IN	9/10	**Receiver Clock:** This input is the 16 x baud rate clock for the receiver section of the chip.
SIN	IN	10/11	**Serial Input:** Serial data input from communication link such as peripheral device, MODEM or data set.
CTS*	IN	36/40	**Clear to send:** When low, this pin indicates that the MODEM or data set is ready to exchange data. The CTS* signal is a MODEM status input whose conditions can be tested by the CPU reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the CTS* signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the CTS* input has changed state since the previous reading of the modem Status Register, CTS* has no effect on the Transmitter. Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
DSR*	IN	37/41	**Data Set Ready:** When low, this pin indicates that the MODEM or data set is ready to establish the communications link with the UART. The DSR* signal is a MODEM status input whose condition can be tested by the CPU reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the DSR signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the DSR* input has changed state since the previous reading of the MOEM status Register. DSR* has no the transmitter. Note: whenever the DSR bit of the MODM Status Register changes state, an interrupt is generates if the MODEM Status Interrupt is enables.
DCD*	IN	38/42	**Data Carrier Detect:** When low, this pin indicates that the data carrier has been detected by the MODEM or data set. The DCD* signal is a MODEM status input whose condition can be tested by the CPU reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the RLSD* signal. Bit 3(DDCD) of the MODEM Status Register indicates whether the DCD* input has changed state since the previous reading of the MODEM Status Register. DCD* has no effect on the receiver. Note: whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status interrupt is enabled.
RI*	IN	39/43	**Ring indicator:** When low, this pin indicates that a telephone ringing signal has been received by the MODEM or data set. The RI* signal is a MODEM status input whose condition can be tested by the CPU reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the RI* signal. Bit 2(TERI) of the MODEM Status Register indicates whether the RI* input signal has changed from a low to a high state since the previous reading of the MODEM Status Register. Note: Whenever the RI bit of the MODEM Status Register changes from a low to a high state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Mnemonic	Pin type	PIN # for 40-DIP/ 44-PLCC	Description
VCC	IN	40/44	+5V supply
VSS	IN	20/22	Ground
DTR*	OUT	33/37	**Data Terminal Ready:** When low, this informs the MODEM or data set that the UART is ready to establish a communication link. The DTR* output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
RTS*	OUT	32/36	**Request To Send:** When low, this informs the MODEM or data set that the UART is ready to exchange data. The RTS* output signal can be set to an active low by programming bit1 (RTS) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop operation holds this signal in its inactive state.
OUT1*	OUT	34/38	**Output 1:** This user-designated output can be set to an active low by programming bit 2 (OUT1) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
OUT2*	OUT	31/35	**Output 2:** This user-designated output can be set to an active low by programming bit 3 (OUT2) of the MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
CSOUT	OUT	24/27	**Chip Select out (CSOUT) pin:** When high, this pin indicates that the chip has been selected by active CS0, CS1, and CS2* inputs. No data transfer can be initiated until the CSOUT signal is a logic 1. This pin goes low when the chip is deselected.
DDIS	OUT	23/26	**Driver Disable:** This goes low whenever the CPU is reading data or status from the UART. It can be used to disable or control the direction of a data bus transceiver between the CPU and the UART.
BAUDOUT*	OUT	15/17	**Baud Out Clock:** this is the 16 x clock signal from the transmitter section of the UART. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The BAYUDOUT* may also be used for the receiver section by tying this output to the RCLK input of the chip.
INTRPT	OUT	30/33	**Interrupt:** This pin goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.
SOUT	OUT	11/13	**Serial Output:** Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

Mnemonic	Pin type	PIN # for 40-DIP/ 44-PLCC	Description
D0-D7	I/O	1:8/2:9	**Data Bus D0-D7:** This 3-state bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D(0:7) Data Bus.
XTAL1, XTAL2	IN, OUT	16/17; 18/19	**External Clock Input/Output:** These two pins connect the main timing reference (crystal or signal clock) to the UART. See Figure 5 for circuit connection diagram (see below).
NC	N	29/1,12,23,32,34	**Pin not connected**

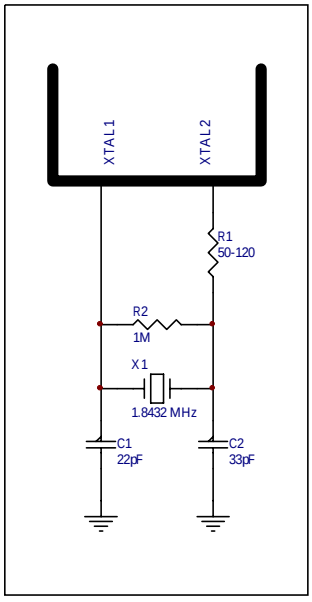


Figure 5: External Crystal Oscillator Connection

UART OPERATION DESCRIPTION

MASTER RESET

A High level input on MR pin resets UART and forces internal register and output pins as shown in Table 1.

TABLE 1-Reset Configuration of Registers and Output Signals

Register/signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All bits low-(bits(4-7) are permanently low)
Interrupt identification Register	Master Reset	Bit 0 is forced high and bit (1-3), 6, 7 are forced low-bits 4 and 5 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low- (bits (5-7) are permanently low)
Line Status Register	Master Reset	All bits low-except bies5, 6which are high
Modem Status Register	Master Reset MODEM Signal inputs	Bits (0-3) low Bits (4-7) follow input signals
SOUT	Master Reset	High
INTRPT (RCVR ERRS)	Master Reset/Read LSR	Low
INTRRPT (RCVR DATA READY)	Master Reset/Read RBR	Low
INTRPT (THRE)	Master Reset/Read IIR/Write THR	Low
OUT2*	Master Reset	High
Out1*	Master Reset	High
RTS*	Master Reset	High
DTR*	Master Reset	High

INTERNAL REGISTER DESCRIPTION

The system programmer has access to any of the registers as summarized in Table II.

Table II – Accessible IMP16C450 Registers

Register Address					
	0DLAB=0	0DLAB=0	1DLAb=0	2	3
Bit no.	Receiver buffer register (Read Only)	Transmitter Holding Register (Write only)	Interrupt Enable Register	Interrupt Idendification Register (Read Only)	Line Control Register
	RBR	THR	IER	IIR	LCR
0	Data Bit 0	Data Bit 0	Enable Data Register Interrupt (ERBFI)	"0" if Received Pending	Word Length Interrupt Select bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty interrupt (ETBE)	Interrupt ID bit 0 (IIDB0)	Word Length Select bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID bit 1 (IIDB1)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	Interrupt ID bit 2(IIDB2)	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	0	Set Break Control
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access bit (DLAB)

Table II – Accessible IMP16C450 Registers (continued)

Register Address						
Bit No.	4	5	6	7	0DLAB=1	1DLAB=1
	MODEM Control register	Line Status Register (Read Only)	MODEM Status Register	Scratch Pad Register	Divisor	Divisor Latch (MSB)
	MCR	LSR	MSR	SCR	DLL	DLM
	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
	Out 1	Parity Error (FE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
	Out 2	Framing Error (FE)	Delta Receive Line Signal Delta (DRLSD)	Bit 3	Bit 3	Bit 11
	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
	0	0	Receive Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via also read the Register (LCR). The programmer can also read contents of the line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

Bits 0 and1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted and received in each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop its are generated. The receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The Parity bit is used to produce an even or odd number of `s when the data word bits and Parity bit are summed).

Bit 4: This bit is the Even Parity Selects bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1`s is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1`s is transmitted or checked in the data word bits and Parity bit.

Bit 5: This bit is the Stick Parity bit. When bits 3 and 5 are logic 1 the parity bit is transmitted and detected by the receiver in the opposite state indicated by bit 4. If bit 5 is zero, Stick parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When bit 6 is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there until bit 6 is set to a logic 0. This bit acts only on SOUT pin and has no effect on transmitter logic. This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous characters will be transmitted because of break.

1. Load an all 0s, pad character, in response to HRE.
2. Set Break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break the Transmitter can be used as a character timer t o accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. Is must be set low (logic 0) to access the receiver Buffer, the Transmitter Holding Register, or the interrupt Enable Register.

Programmable Baud Rate Generator

The UART contains a programmable Baud Generator that is capable of taking any clock input from DC to 8.0 MHz and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches operation of the Baud Rate Generator. Upon loading either of the Divisor latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load.

Table III, IV and V illustrate the use of the Baud Rate Generator with three different driving frequencies. Table III references to a 1.8430 MHz clock, table IV to a 3.070 MHz clock, and table V to a 8 MHz clock. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is not recommended. In no case should the data rate be greater than 512K baud

TABLE III-Baud Rates Using 1.8432 MHz clock

Desired Baud Rate	Divisor Used to generate 16 x clock	Percent Error Difference Between Desired and Actual
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.690
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2(*)	2.860

TABLE IV-Baud Rate using 3.072 MHz clock

Desired Baud Rate	Divisor Used to generate 16 x clock	Percent Error Difference Between Desired and Actual
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.230
9600	20	-
19200	10	-
38400	5	-
56000	3(*)	14.285

TABLE V-Baud Rate using 8.0 MHz Clock

Desired Baud Rate	Divisor Used to generate 16 x clock	Percent Error Difference Between Desired and Actual
50	10000	-
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	-
2400	208	1.160
3600	139	0.080
4800	104	1.160
7200	69	0.644
9600	52	1.160
19200	26	1.160
38400	13	1.160
56000	9	0.790
128000	4	2.344
256000	2(*)	2.344

(*) smallest allowable divisor when using corresponding crystal.

Line Status Register

This register provides status information to the CPU concerning the data transfer. Table II shows the contents of the Line Status Register. Description of each bit follows:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, there by destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character doses not have the correct even or odd parity, as selected by the even-parity -select bit. The PE is set to a logic 2 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a logic 0 bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line status Register. The UART will resynchronize after a Framing Error.

Bit 4: This bit is the Break interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads

the contents of the Lines Status Register.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register..The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or the TSR contains a data character.

Bit 7: This bit is always logic 0.

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels, The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1),Received Data Ready (priority @),Transmitter Holding Register Empty (priority 3),and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the interrupt identification Register. Register IIR, when addressed during chip select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Its contents are indicated in Table VI and are described below:

Bit 0: This bit can be used in a prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bit 1,2: These two bits of the IIR are used to identify the highest priority interrupt pending (see Table VI).
Bit 3-7: these bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the UART to separately activate the chip interrupt (INTRPT) output signal. Each interrupt can individually activate the interrupt (INTRPT) output signal. Its contents are indicated in Table II and are described below. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INTRPT output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers.

Bit 0: This bit enables the Received Data Available interrupt set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bit 4-7: These four bits are always logic 0.

Scratch Pad Register

This 8-bit Read/Write Register does not control the UART in anyway. It is intended as a scratch pad register to be used by the programmer to hold general purpose data temporarily.

TABLEL VI-Interrupt Control Functions

Interrupt Identification Register					Interrupt Set and Read Functions	
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to send or Data Set ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM status Register

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM control Register are indicated in Table II and are described below:

Bit 0: This bit controls the Data Terminal Ready (DTR) output. When bit 0 is set to a logic 1, the DTR output is forced to a logic 0. When bit 0 is reset to a logic 0, the DTR output is forced to a logic 1.

Note: The DTR output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM OR data set.

Bit 1: This bit controls the Request to Send (RTS*) output. Bit 1 affects the RTS output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 (OUT 1) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1 output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 (OUT2) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT2 output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic 1 (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM Control inputs (CTS, DSR, RLSD and RI*) are disconnected, and the MIDEM Control output pins (RTS, DTR, OUT2 and OUT1*) are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and receive-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupt are fully operational, The MODEM control Interrupts are also operational. The MODEM control Interrupts are also operational, but the sources of interrupts are now the lower four bits of the MODEM Control Register instead fo the four MODEM control inputs. The interrupts are still controlled by the interrupt Enable Register.

Bit 5-7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM or data set (or a peripheral device emulating a modem) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.
The contents of the MODEM Status Register are indicated in Table II and described below:

Bit 0: This bit is the delta Clear to Send (DCTS) indicator. Bit 0 when set to logic 1, indicates that the CTS input to the chip has changed state since the last time this bit was cleared to logic 0 by reading this bit by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator, Bit 1 when set to logic 1, indicates that the DSR input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Rin Indicator (TREI) detector. Bit 2 indicates that the RI input to the chip has changed from a low to high state since the last time it was read by the CPU.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 when set to logic 1, indicates that the DCD* input to the chip has changed state since the last time it was read by the CPU.

Note: Whenever bit 0,1,2, or 3 is set to logic 1, a MODEM Status Interrupt is generated, if bit 3 (EDSSI) of the interrupt enable register is set.

Bit 4: This bit is the complement of the Clear to Send (CTS*) input. This bit is equivalent to bit RTS of the MODEM control register, if bit 4 of the MCR is set to (loop mode).

Bit 5: This bit is the complement of the Data Set Ready (DSR*) input. This bit is equivalent to bit DTR of the MODEM control register, if bit 4 of the MCR is set to 1(loop mode).

Bit 6: This bit is the complement of the Ring Indicator (RI) input. This bit is equivalent to bit OUT1 of the MODEM control register, if bit 4 the MCR is set to 1 (loop mode).

Bit 7: This bit is the complement of the Received Line Signal Detect (RLSD*) input. This bits equivalent to bit OUT2 of the MODEM control register, if bit 4 of the MCR is set to 1 (loop mode).

AC, DC TIMING SPECIFICATION

Absolute Maximum Ratings

Temperature Under Bias	0^0c to $+70^0$c
Storage or Output Voltage	-65^0c to $+150^0$c
All Input or Output Voltages With Respect to VSS 0^0c	-0.5^0c to $+7.0^0$c
Power Dissipation	1W

If Military/Aerospace specified devices are required. contact Modular for availability and specifications. Note: Maximum rating indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

TA=0^0C to + 70^0c, Vcc=+5V±5%, Vss=0V, unless otherwise specified

Symbol	Paramater	Conditions	Min	Max	Units
VILX	Clock Input Low Voltage		-0. 5V	0.8	V
VIHX	Clock Input High Voltage		2. 0	Vcc	V
VIL	Input Low Voltage		-0. 5V	0.8	V
VIH	Input High Voltage		2. 0	Vcc	V
VOL	Output Low Voltage	IOL = 2 mA on all (note 1)		0.4	V
VOH	Output High Voltage	Loh = -1. 0 mA (note 1)	2. 4		V
ICC(AV)	Avg. Power Supply Current(Vcc)	Vcc =5. 25V, f=8MHz No Loads on outputs SIN, DSR, DCD CTS, RI=2. 0V all other inputs =0. 8V		10	mA
IIL	Input Leakage	Vcc=5. 25V, Vss=0V all other pins floating		±10	µA
ICL	Clock Leakage	VOUT =0V, 5. 25V		±10	µA
LOZ	Tri-State® Leakage	VCC=5. 25V, VSS=0V VOUT =0V, 5. 25V 1) chip deselected 2) WRITE mode,chip selected		±10	µA
VILMR	MR Schimitt VIL			0. 8	V
VIHMR	MR Schmitt VIH		2. 0		V

(note 1) Does not apply to XOUT

CAPACITANCE

TA=25^0C,VCC=VSS=0V

Symbol	Paramater	Condltions	Min	Typ	Max	Units
CXIN	Clock Input Capacitance			15	20	pF
CXOUT	Clock Output Capacitance	Fc =1 MHz		20	30	pF
CIN	Input Capacitance	Unmeasured pins		6	10	pF
COUT	Output Capacitance	Returned to VSS		10	20	pF

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