Quad Universal Asynchronous Receiver/Transmitter (UART)

FIFO Counter & 128-BYTE FIFO

Description

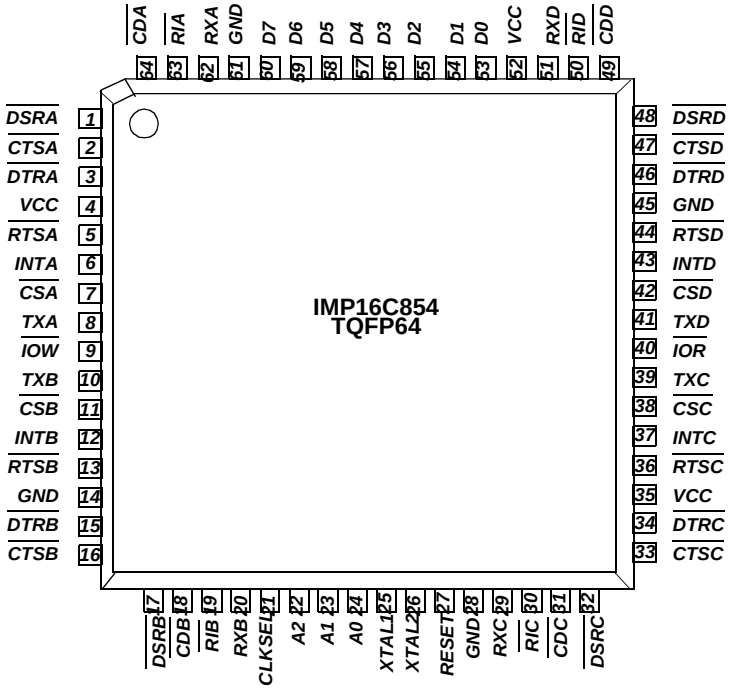
The IMP16C854 is a universal asynchronous receiver and transmitter (UART) and is available in different packages. The IMP16C854 is an quad UART with enhanced features like 128 byte deep transmit and receive fifo's, programmable transmit and receive trigger levels to enable data rates of 2Mbps with low system interface overhead and in band/out of band flow controls. Status registers provide the user with error indications and operational status, modem interface control status. Interrupt levels are software programmable to suit different system requirements. Internal loopback capability facilitates diagnostics. Low power modes of IMP16C854 enables its use in critical low power applications.

The IMP16C854 is available in industry standard 64 pin TQFP, 68 pin PLCC and 100 pin QFP packages. Each additional pin on the package makes available additional range of features for the application.

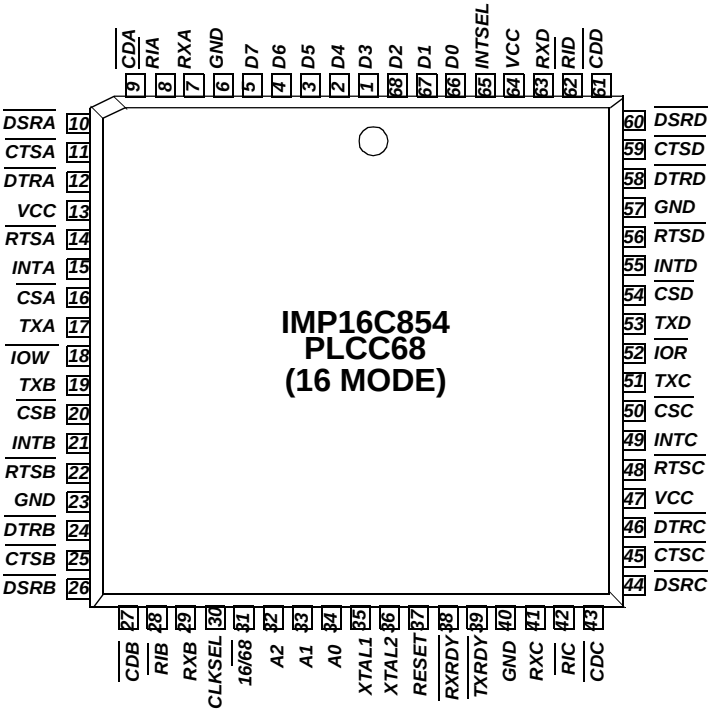
Key Features

- Compatibility with the Industry Standard ST16C454, ST68C454, ST68C554, TL16C554, ST16C654, ST68C654, TL16C554FN and TL16C754FN.
- Data Rates upto 2Mbps.
- 128 byte transmit FIFO and receive fifo.
- Programmable FIFO interrupt Generation.
- CTS/RTS flow control with Hysteresis.
- Xon/Xoff flow control.
- Selectable clock frequency pre-scaler and programmable baud rate generator.
- IrDA v1.0 encoder/decoder interface along with standard wired modem interface.
- Low power mode.
- 3.3V operation.

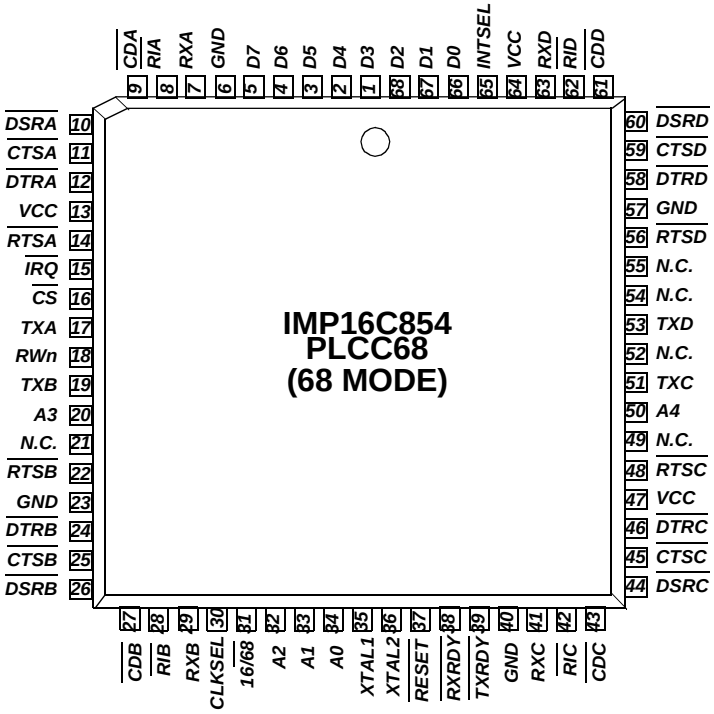
Pin Description



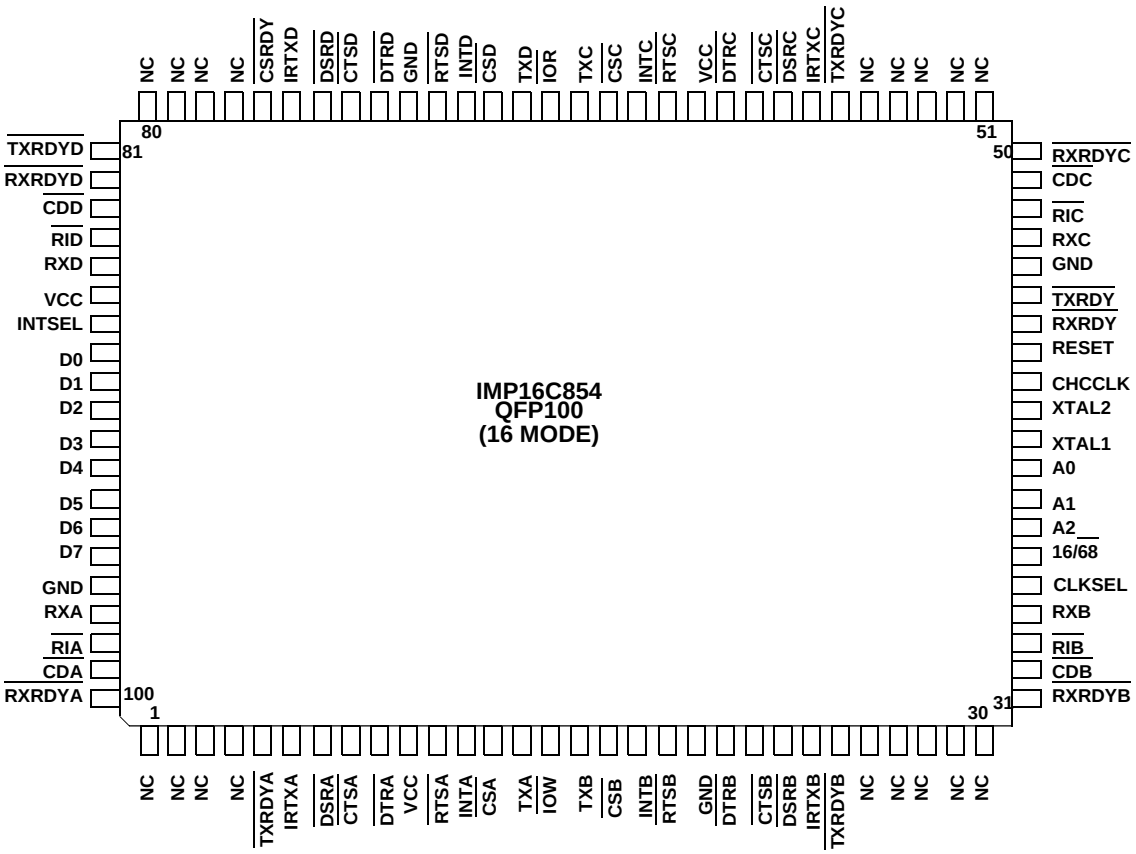
64-pin TQFP Package Signals



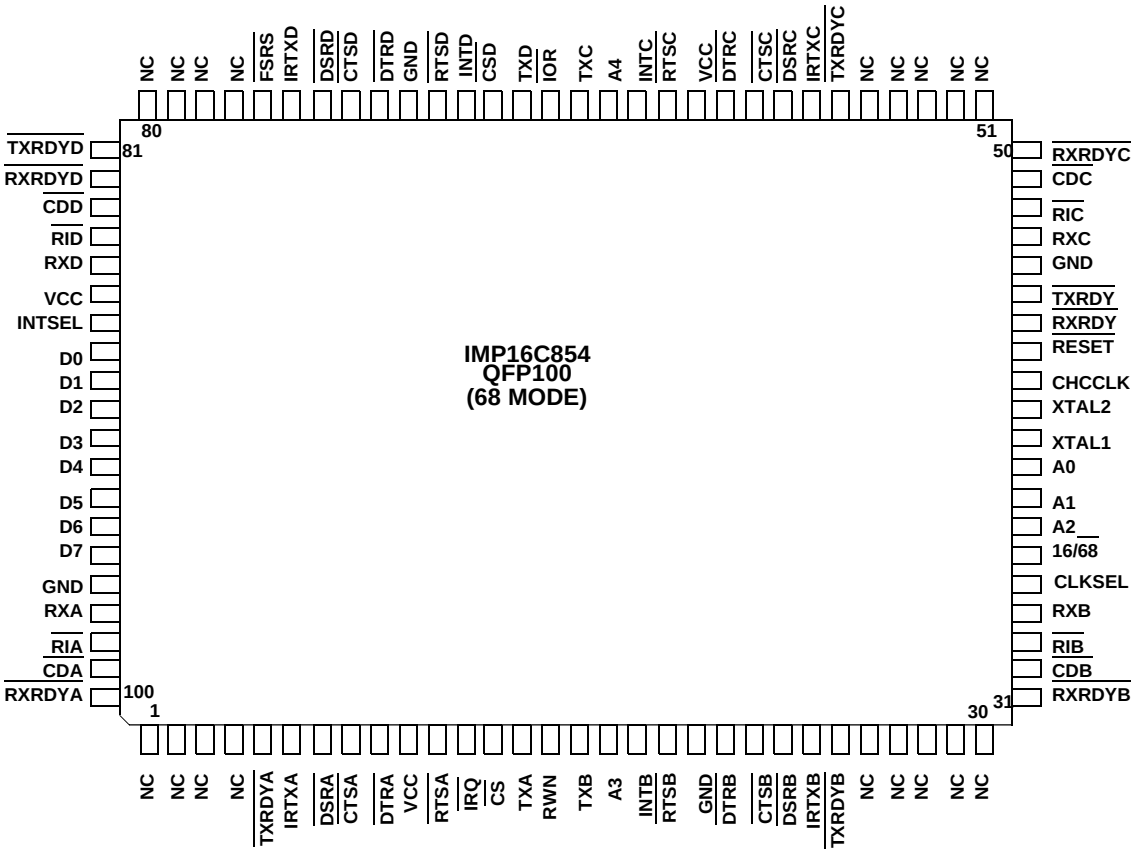
68-Pin PLCC Package Signals in 16 mode



68-Pin PLCC Package Signals in 68 mode



QFP100 Package Signal in 16 mode



QFP100 Package Signals in 68 mode

Table 1 : Signal Description

Symbol	Pin			Type	Pin Description
	PLCC68	TQFP64	QFP100		
NC	-	-	1-4, 26-30, 51-55, 77-80	-	No Connect.
GND	6,23, 40,57	14,28, 45,61	20,46, 71,96		Ground.

Table 1 : Signal Description

Symbol	Pin			Type	Pin Description
	PLCC68	TQFP64	QFP100		
VCC	13,47 64	4, 35,52	10,61 86		Power
XTAL1	35	25	40	I	Crystal or External Clock Input - Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates.
XTAL2	36	26	41	O	Output of the Crystal Oscillator or Buffered Clock - Crystal oscillator output or buffered clock output.
RESET/$\overline{\text{RESET}}$	37	27	43	I	Reset. - In the intel processor interface mode, this is active high reset for the IMP16C854. In motorola interface mode, this is active low reset for the IMP16C854.
CLKSEL	30	21	35	I	Clock Select (input with internal pullup) - This pin selects the clock pre-scaler. If connected to logic 1, the input clock is selected. If connected to logic 0, divide by 4 clock is selected. MCR bit 7 can override this state following reset or initialization.
CPU Interface Signals					
16/$\overline{68}$	31	-	36	I	16/68 Interface Type Select (input with internal pull-up). This input selects CPU interface to be 16 (Intel) or 68 (Motorola) bus interface. The functions of $\overline{\text{IOR}}$, $\overline{\text{IOW}}$,INT A-D, and -$\overline{\text{CS}}$ A-D are re-assigned with the logical state of this pin. When this pin is a logic 1, the intel type CPU bus interface is selected. When this pin is a logic 0, the motorola type CPU bus interface is selected. This pin is not available on 64 pin packages which allows only intel type CPU bus interface.
A0,A1,A2	34,33,32	24,23,22	39,38,37	I	Address-0-2 Inputs are used to select a specific internal register of one of the four UARTs for read/write access.
$\overline{\text{CSA}}$/$\overline{\text{CS}}$	16	7	13	I	Chip Select. (active low) - In the motorola bus interface mode, this pin functions as a chip enable. In this case, all four UARTs are enabled when the $\overline{\text{CS}}$ pin is a logic 0. An individual UART channel is selected by the address bits A3-A4. When the intel bus interface mode is selected, this pin functions as $\overline{\text{CSA}}$, selecting UART channel A registers for read/write accesses.
$\overline{\text{CSB}}$/A3	20	11	17	I	Chip Select (active low) - In motorola bus interface mode, this pin provides one of the two additional address lines required to select one of the 4 UARTs in the IMP16C854. In Intel bus interface mode, this active low input selects UART channel B registers for read/write accesses.
$\overline{\text{CSC}}$/A4	50	38	64	I	Chip Select (active low) - In motorola bus interface mode, this pin provides one of the two additional address lines required to select one of the 4 UARTs in the IMP16C854. In Intel bus interface mode, this active low input selects UART channel C registers for read/write accesses.
$\overline{\text{CSD}}$	54	42	68	I	Chip Select (active low) - In motorola bus interface mode, this pin is a No Connect. In Intel bus interface mode, this active low input selects UART channel D registers for read/write accesses.

Table 1 : Signal Description

Symbol	Pin			Type	Pin Description
	PLCC68	TQFP64	QFP100		
D0-D7	66-5	53-60	88-95	I/O	Data Bus (Bi-directional) - These are the eight bit, bidirectional data bus for transferring information to or from the controlling application.
INTSEL	65	-	87	I	Interrupt Select. (active high, with internal pull-down) - When the intel bus interface mode is selected, this pin can be used in conjunction with MCR bit-3 to enable or disable the tri-stating of the interrupt outputs for each of the channels. Interrupt outputs are enabled continuously by connecting this pin to a logic 1. Connecting this pin to a logic 0 allows MCR bit-3 to control the three state interrupt output. In this mode, MCR bit-3 is set to a logic 0 to enable the three state outputs. This pin must be connected to logic 0 in motorola bus interface mode. Since this pin is not available in TQFP64 package, two different versions are available. In IMP16C854D, operates in continuous interrupt mode, while the IMP16C854 the interrupt pin function is controlled by MCR bit 3.
$\overline{IOR}$	52	40	66	I	Read strobe. (active low Strobe) - This function is associated with the intel bus interface mode only. A logic 0 transition on this pin will load the contents of an Internal register defined by address bits A0-A2 onto the data bus (D0-D7) for access by an application. This pin is NC in motorola bus interface mode.
$\overline{IOW}$/RWn	18	9	15	I	Write strobe. (active low strobe) - In intel bus interface mode, a logic 0 transition on this pin will transfer the contents of the data bus (D0-D7) from the application to an internal register that is selected. In motorola bus interface mode, this pin acts as active high read strobe or active low write strobe.
INTA/$\overline{IRQ}$	15	6	12	O	Interrupt A/ $\overline{IRQ}$ - In Intel bus interface mode, this pin is active high and goes active if any one of the enabled causes of interrupts in the channel A UART is requiring application attention. Its going high is also controlled by INTSEL and MCR bit 3. In motorola bus interface mode, this pin is active low and goes active if any one of the enabled causes of interrupts in any of the 4 UART channels is requiring applications attention. INTSEL must be grounded for this pin to work properly in motorola bus interface mode.
INTB, INTC, INTD	21,49,55	12,37,43	18,63,69	O	Interrupt B, C, D (active high) - This function is associated with the intel bus interface mode only. These pins provide individual channel interrupts, INT B-D. INT B-D are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. In motorola bus interface mode, these pins are NC's.
$\overline{FSRS}$	-	-	76	I	Active low FIFO Status Register Select (internal pull-up) - When low, selects the FIFO status register for read. The address and the CS signals are not used when this signal is active low.
$\overline{RXRDY}$	38	-	44	O	Receive Ready (active low) - This function is associated with 68/100 pin packages only. $\overline{RXRDY}$ when low indicates that at least one channel receive FIFO contains received data. This pin goes to a logic 1 when the FIFO/RHR is empty. For 64/68 pin packages, individual channel RX status is read by examining individual internal registers using $\overline{CS}$ and A0-A4 pin functions.

Table 1 : Signal Description

Symbol	Pin			Type	Pin Description
	PLCC68	TQFP64	QFP100		
$\overline{TXRDY}$	39	-	45	O	Transmit Ready (active low) - This function is associated with 68/100 pin package only. $\overline{TXRDY}$ when 0 indicates a buffer ready status, i.e., at least one location is empty and available in one of the TX channels (A-D). This pin goes to a logic 1 when all four channels have no more empty locations in the TX FIFO or THR.
$\overline{RXRDYA}$, $\overline{RXRDYB}$, $\overline{RXRDYC}$, $\overline{RXRDYD}$	-	-	100, 31, 50,82	O	Receive Ready (active low) - These pins are available on QFP100 package only. When low, indicates at least one byte available in receive FIFO for the application to read. Signal goes high when there are no bytes in the receive fifo or the number of bytes in the receive fifo falls below the programmed trigger level.
$\overline{TXRDYA}$, $\overline{TXRDYB}$, $\overline{TXRDYC}$, $\overline{TXRDYD}$	-	-	5, 25, 56, 81	O	Transmit Ready (active low) - These pins are available on QPF100 package only. When low it indicates that there is at least 1 empty/free location in the transmit FIFO. It goes high when all locations in the transmit FIFO are full.
CHCCLK	-	-	42	I	Channel C Clock - This pin is available on QFP100 package only. This pin provides the clock for UART channel C. An external clock or XTAL2 must be connected to this pin for normal operation.
Serial Interface Signals					
$\overline{CDA}$, $\overline{CDB}$, $\overline{CDC}$, $\overline{CDD}$	9,27, 43,61	64,18, 31,49	99,32, 49,83	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through D. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CTSA}$, $\overline{CTSB}$, $\overline{CTSC}$, $\overline{CTSD}$	11,25 45,59	2,16 33,47	8,22, 59,73	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on the CTS pin indicates the modem or data set is ready to accept transmit data from the 554D. Status can be tested by reading MSR bit-4. When auto hardware flow control function is enabled, this inputs when low enables the transmitter and when high, disables the transmitter from transmitting any further characters after the current character transmission is completed.
$\overline{DSRA}$, $\overline{DSRB}$, $\overline{DSRC}$, $\overline{DSRD}$	10,26 44,60	1,17 32,48	7,23, 58,74	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UARTs transmit or receive operation.
$\overline{RIA}$, $\overline{RIB}$, $\overline{RIC}$, $\overline{RID}$	8,28 42,62	63,19 30,50	98, 33, 48,84	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt.
$\overline{DTRA}$, $\overline{DTRB}$, $\overline{DTRC}$, $\overline{DTRD}$	12,24 46,58	3,15 34,46	9,21, 60,72	O	Data Terminal Ready (active low) - These inputs are associated with individual UART channels, A through D. A logic 0 on this pin indicates that the 554D is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR bit-0 will set the $\overline{DTR}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0. This pin has no effect on the UARTs transmit or receive operation.

Table 1 : Signal Description

Symbol	Pin			Type	Pin Description
	PLCC68	TQFP64	QFP100		
$\overline{RTSA}$, $\overline{RTSB}$, $\overline{RTSC}$, $\overline{RTSD}$	14,22 48,56	5,13 36, 44	11,19, 62,70	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through D. A logic 0 on the $\overline{RTS}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin has no effect on the UARTs transmit or receive operation. When auto hardware flow control is enabled, this output is controlled by the receive FIFO levels, trigger levels and the RTS hysterisis programmed.
RXA, RXB, RXC, RXD (IRRXA, IRRXB, IRRXC, IRRXD)	7,29 41,63	62,20 29,51	97,34, 47,85	I	Receive Data Input RX A-D. - These inputs are associated with individual serial channel data input to the IMP16C854D. During the local loopback mode, the RX input pin is disabled and TX data is internally connected to the UART RX Input, internally. MCR bit 6 controls the mode for this pin.
TXA, TXB, TXC, TXD (IRTXA, IRTXB, IRTXC, IRTXD)	17,19 51,53	8,10 39,41	14,16, 65,67 (6,24, 57,75)	O	Transmit Data - These outputs are associated with individual serial transmit channel data. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX Input. In QFP100 package, TX and IRTX both pins are available while in other packages the MCR bit 6 selected the mode.

General Description

The IMP16C854 provides quad serial asynchronous transmit / receive functionality. It performs parallel to serial data conversion and frames each character according to programmed parameters. It also performs the serial to parallel data conversion after stripping of the framing bits from the characters. While framing the character, the transmitter adds start and stop bits and the parity bit for checking data integrity according to programmed parameters. The receiver strips the start and the stop bits and checks for character integrity by checking the parity bit if programmed.

The IMP16C854 provides easy interface to both motorola and intel processors. This is achieved by additional onboard logic that enables glueless interface to both intel and motorola processor busses. The IMP16C854 is capable of data transfers at 1.5 Mbps on each channel. It provides modem interface status/control inputs and outputs for easy of interface to modems. It provides independent baud rate generator for each channel.

The IMP16C854 is an upward solution that provides 128 bytes of transmit and receive FIFOs and can be software configured to work as 16C554/16C654 or 16C754. The 854D is designed to work in application environments that required high throughput. By providing deeper transmit and receive FIFO's and auto flow control features the IMP16C854 successfully allows increased latency in application servicing a request from the UARTs without loosing any data. Programmable trigger levels for transmit and receive fifo's provide additional option to fine tune the system to provide optimal performance.

The IMP16C854 also provides a pre-scales which can select the input clock frequency to 1X or 4X depending on the state of CLKSEL input and the MCR bit 7. It also provides an external clock option which allows connection to a external MIDI oscillator for MIDI interface. The IMP16C854 also provide IrDA outputs for use in wireless applications. Loop-

back modes allow diagnostic of the hardware to locate faults quickly. In addition, the IMP16C854 provides low power mode to enable its use in low power UART applications.

The IMP16C854 is available if various packages and bonding options to allow multiple footprints to be supported in application environment. These footprints are compatible to industry standard parts offered by other vendors.

Functional Description

The Intel Bus Interface Mode

The intel bus interface mode is enabled by connecting 16/$\overline{68}$ pin to high. This enables the IMP16C854 to interface easily with the intel processor bus interface. Each UART is selected with its individual chip select ($\overline{CSA}$, $\overline{CSB}$, $\overline{CSC}$, $\overline{CSD}$) pins. When selected, the UARTs respond according to the state of $\overline{IOW}$ and $\overline{IOR}$ signals.

The Motorola Bus Interface Mode

The motorola bus interface mode is enabled by connected the 16/$\overline{68}$ pin to a logic low. In this mode, the individual UARTs are selected by a common select input and the address inputs A3,A4 according to the table shown below. The RWn input determines if the current bus cycle is read or write.

Table 2 : UART Channel Selection, Motorola Mode Interface

$\overline{CS}$	A4	A3	UART Channel
1	X	X	None
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D

Internal Registers

The IMP16C854 provides 21 internal registers per channel for monitoring and control of UART channels. These resisters are shown in Table below. These registers are similar to those already available in the standard 16C554/16C654. These registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), FIFO control register(FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable baud rate registers (DLL/DLM), and a general purpose scratch pad register (SPR). Additional registers include enhanced feature registers EFR, Flow control character registers, FCTR, Trigger level register, and EMSR. The following table shows the register map. Refer to register description section for further details on individual registers.

Table 3 : Internal Register

A2	A1	A0	Read Mode	Write Mode
General Registers accessible only when LCR is not 0xBF				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Factory Test Register
1	1	0	Modem Status Register	NA
1	1	1	Scratch Pad Register	Scratch Pad Register
1	1	1	FIFO Level Counter Register[a]	Enhanced Mode Select Register[b]
Baud Rate Register Set (DLL/DLM) accessible when LCR[7] = 1 and LCR is not 0xBF				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Enhanced Register accessible only when LCR is 0xBF				
0	0	0	FIFO Level Counter	FIFO Trigger Level
0	0	1	Feature Control Register	Feature Control Register
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon-1 Byte	Xon-1 Byte
1	0	1	Xon-2 Byte	Xon-2 Byte
1	1	0	Xoff-1 Byte	Xoff-1 Byte
1	1	1	Xoff-2 Byte	Xoff-2 Byte
FIFO Status Register (Accessed when $\overline{\text{FSRS}}$ is active.)				
x	x	x	FSR	NA

a. Register available only when FCTR[6] set to 1.
b. Register available only when FCTR[6] set to 1.

Flow Control

The IMP16C854 allows both in-band and out-of-band flow control. This is explained in detail in the text below.

in-band Flow Control

The IMP16C854 can control the flow of data on the serial interface using the TX/RX lines. When enabled, the receiver compares one or two sequential characters received with the programmed Xon/Xoff characters. If a match is found to the programmed Xoff characters, the transmitter will pause data transmission as soon as the current character is completely transmitted. The receiver continues to monitor the Rx input and when a match is found to the programmed Xon characters, the transmitter will resume the transmit operation starting from the next data byte in the FIFO. The happening of these events can also be indicated to the application by generating an interrupt if programmed to do so. Both the Xon/Xoff characters are user programmable.

A special Xon mode is also available in IMP16C854. Subsequent to pausing transmission because of xoff character reception, the transmitter can resume transmission as soon as the receiver receives any character.

Similarly while receiving data, if in-band flow control is enabled, an xoff character is sent by the transmitter when the receive fifo contains two byte over the programmed trigger level to indicate to the remote device to pause transmission. When the receive fifo level falls below the trigger level, the transmitter transmits Xon character/s to indicate to the remote device to resume transmission. Various options available for in-band flow control are described in the EFR register description. The IMP16C854 also provides a mode in which the received XOFF/XON characters are transferred to receive FIFO like any other character.

While comparing the incoming characters with the programmed XON/XOFF characters, only the programmed number of bits per character are compared. This is controlled by LCR bits 0-1.

Out-Of-Band Flow Control

The IMP16C854 can be programmed to achieve data flow control using RTS/CTS signals. In this case, the RTS output pin is used to request remote unit to pause/resume transmission while the CTS input pin is monitored to control the local transmission. When the data in the receive FIFO exceeds the programmed trigger level, the RTS pin is deasserted. This is connected to remote CTS pin which indicates to the remote transmitter to stop transmission. When the data in receive fifo falls below the trigger level, the RTS pin is reasserted and the remote transmitter resumes transmission. The local transmitter stops transmission when the local CTS input is deasserted after completing the current character transmission. It resumes transmission when the CTS pin reasserts. Interrupts can be generation on a change of state on the CTS/RTS pins to inform the application about the status of the transmitter/receiver.

In order to increase the through put, the IMP16C854 provides RTS hysteresis. This allows the RTS to deactivate programmed number of bytes after trigger level has reached. Once RTS deactivates, it reactivates after the RxFifo level reaches programmed number of bytes below the trigger level. This feature enables fine tuning the system throughput in different application environments.

Interrupts

The device contains 128 deep byte wide transmit fifo and 128 deep 11 bit wide receive fifo. The receive fifo also stores the error conditions. The IMP16C854 includes programmable trigger levels for the transmit fifo also and the interrupt can be generated according to these programmed trigger levels. Same is true with the receive fifo.

In addition, the receive fifo has a logic that generates time-out interrupt if the receive FIFO contains data but the number of bytes is less than the programmed trigger level and there is no activity at the FIFO input/output for 4 consecutive character time. This enables the application the handle the end of a receive packet successfully without any latency in receiving a complete packet or loosing received data.

Each UART provides seven interrupts. The transmit holding interrupt is generated whenever the transmit FIFO is empty if the interrupt is enabled. This interrupt is disabled when the interrupt status register is read or transmit FIFO is loaded with new data. The receive data interrupt is generated when the receive fifo level reaches the programmed trigger level. The receiver also provide the time-out interrupt which has been described above. In addition it also provides the line status interrupt cause by an error condition being observed in the receiver which can be because of parity incorrectness, framing incorrectness, overrun or break detection on the Rx input. Any change in modem status inputs can also cause an interrupt to be generated. Other two interrupts can be generated by the auto flow control is enabled and an flow control option is exercised during transmission or reception of data. Each of the interrupt conditions mentioned above are individually maskable.

The interrupt outputs can be controlled according to system requirements. The system/ board designer can optionally use software controlled three state interrupt operation. This is accomplished by INTSEL and MCR bit-3. When INTSEL interface pin is left open or made a logic 0, MCR bit-3 controls the three state interrupt outputs, INT A-D. When INTSEL is a logic 1, MCR bit-3 has no effect on the INT A-D outputs and the package operates with interrupt outputs enabled continuously.

Programmable Baud Rate Generator

Single baud rate generator per UART channel is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator can work with an input clock up to 24 MHz. It can be configured for internal or external clock operation. For internal clock oscillator operation, an industry standard microprocessor crystal (parallel resonant/ 22-33 pF load) is connected externally between the XTAL1 and XTAL2 pins (see figure 8). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal baud rate generator for standard or custom rates.

The generator divides the input 16X clock by any divisor from 1 to 2^{16}-1. The device divides the basic crystal or external clock by 16. Further division of this 16X clock provides two table rates to support low and high data rate applications using the same system design. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator. Using the CLKSEL input, a prescaler that divides the input clock by 4 or 1 can be selected to achieve wide range of baud rates.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table below, shows the two selectable baud rate tables available when using a 7.3728 MHz crystal.

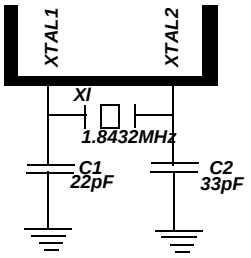


Figure 8: Crystal oscillator connection

Table 4 : DLL / DLM values for different Baud Rates

Output Baud Rate (1.8432 MHz Clock)	Output Baud Rate (7.3728 MHz Clock)	User 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	200	2304	900	09	00
300	1200	384	180	01	80
600	2400	192	C0	00	C0
1200	4800	96	60	00	60
2400	9600	48	30	00	30
4800	19.2K	24	18	00	18
9600	38.4K	12	0C	00	0C
19.2K	76.8K	6	06	00	06
38.4K	153.6K	3	03	00	03
57.6K	230.4K	2	02	00	02
115.2K	460.8K	1	01	00	01

DMA Operation

The IMP16C854s deeper FIFO levels allow effective use of the DMA for block transfer of data to/from UART. When the FIFO is enabled and the DMA mode is also enabled, the application can use the RXRDY and TXRDY to transfer block data from /to the individual uart. When DMA mode is enabled, the RXRDY goes low when the programmed receiver trigger level is reached or a receive time-out has occurred. Once activated, the RXRDY will go high only when there are no more characters in the receive FIFO. This facilitates the use of RXRDY for DMA block transfer of data from the UART to the system memory. Similarly when DMA mode is enabled, the TXRDY goes low when at least 1 byte in the FIFO is empty and goes high when the FIFO is full. This facilitates the use of TXRDY output for DMA block transfers of data to the transmit FIFO.

Low Power Mode

The IMP6C854 allows the control of low power mode for the device by the software. If enabled by a write to IER, the device goes into low power mode. The device will not go into lowe power mode if any interrupt causing condition is active. The device automatically wake up when it detects the start bit or a change of state on modem status inputs or transmit data provided by the application. The device will return to low power mode of operation when the last data byte is read from the receive fifo or the last data byte for transmit has been transmitted.

Loopback Mode

The internal loopback capability allows onboard diagnostics. In the loopback mode the normal modem interface pins are disconnected and reconfigure for loopback internally. MCR register bits 0-3 are used for controlling loopback diagnostic testing. In the loopback mode OP1 and OP2 in the MCR register (bits 3/2) control the modem RI and CD inputs respectively. MCR signals DTR and RTS (bits 0-1) are used to control the modem CTS and DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally. The CTS, DSR, CD, and RI are disconnected from their normal modem control input pins, and instead are connected internally to DTR, RTS, OP1 and OP2. Loopback test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

Register Description

The following description provide details of the different registers in the IMP16C854, the bits in the registers and their functionality.

THR - Transmit Holding Register
Register address: 3'b000.
Post Reset Condition: 0xXX.
Register Access Condition: LCR != 0xBF.

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Table 5 : Transmit Holding Register Bits

Bit	Signal	R/W	Description
7:0	Transmit Data Byte	W	The register holds the transmit data prior to transmission. The status of this register is reflected in the LSR bit 5. Writing to the THR transfers the contents of the data bus (D7-D0) to the THR. If FIFO is enabled, a write to this location transfers the data to the fifo. A write to the register should not be attempted when the LSR bit 5 is low, indicating the THR/FIFO is full.

RHR - Receive Holding Register
Register address: 3'b000.
Post Reset Condition: 0xXX.
Register Access Condition: LCR != 0xBF.

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Table 6 : Receive Holding Register Bits

Bit	Signal	R/W	Description
7:0	Received Data Byte	R	The register holds the received data prior to application reading the byte. The status of this register is reflected in the LSR bit 0.

Register Name: **IER - Interrupt Enable Register**
Register address: 3'b001.
Post Reset Condition: 0x00
Register Access Condition: LCR!= 0xBF

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Table 7 : Interrupt Enable Register Bits

Bit	Signal	R/W	Description
0	RHR Interrupt Enable	RW	This bit when high enables a received byte to generate a interrupt to the application when FIFO is not enabled. When FIFO is enabled and it reaches the trigger level, and interrupt is generated if this bit is set.
1	THR Interrupt Enable	RW	This bit when set and the transmit FIFO level falls below the programmed trigger level, a interrupt is generated for the application. If FIFO is not enabled, the THR empty condition will generate and interrupt for the application.
2	Rx Line Status Interrupt Enable	RW	This bit when set enables any receive error condition to generate an interrupt for the application. These errors can be framing error, parity error, overrun error or break error.
3	Modem Status Interrupt Enable	RW	This bit when set enables a change in modem status inputs to generate an interrupt for the application.
4	Sleep Mode Enable	RW	Can be read/written only if EFR[4] = 1. When set, it enables the device to go into sleep mode. The device cannot go into sleep mode if any interrupt conditions are pending. The device awakes from sleep mode when it detects data write to the transmit holding register or receiver detects a start bit or any of the modem status inputs changes state.
5	Xoff Interrupt Enable	RW	Can be read/written only if EFR[4] = 1. When set, it enables the device to generate an interrupt when the receiver receives an Xoff byte.
6	RTS Output Interrupt Enable	RW	Can be read/written only if EFR[4] = 1. Enables generation of an interrupt when RTS pin transitions from logic 0 to logic1 when set.

Table 7 : Interrupt Enable Register Bits

Bit	Signal	R/W	Description
7	CTS Input Interrupt Enable	RW	Can be read/written only if EFR[4] = 1. Enables generation of an interrupt when CTS pin transitions from logic 0 to logic1 when set.

Register Name: **FCR -FIFO Control Register**
Register address: 3'b010.
Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF.

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Table 8 : FIFO Control Register Bits

Bit	Signal	R/W	Description
0	FIFO Enable	W	This bit when high enables the fifos for receive and transmit data. When low, it disables the FIFO. Note that the bit must be high when any access to the other FCR bits is made.
1	RX Fifo Reset	W	This bit when set clears the receive fifo. The character in the receive shift register is not cleared. This is a auto clear bit and is cleared by the device when the Rx FIFO is cleared.
2	Tx Fifo Reset	W	This bit when set clears the transmit fifo. The character in the transmit shift register is not cleared. This is a auto clear bit and is cleared by the device when the Tx FIFO is cleared.
3	DMA Mode Select	W	This bit selects the DMA mode. This bit controls the operation of TXRDY and RXRDY pins. When this bit is low, the TXRDY goes low when there are no characters in the THR/TxFIFO and goes high when at least one byte is loaded into the THR/TxFIFO. The RXRDY goes low when there is at least 1 byte in the RxFifo/RHR. It will go high when there are no more bytes in the RHR/RxFIFO. When this bit is high, the TXRDY goes low when the THR/TxFIFO has at least one byte empty and goes high when the TXFIFO is full. The RXRDY goes low when the programmed trigger level is reaches or receive time-out occurs and goes high when there are no more characters in the receive FIFO.
4-5	Tx Trigger Select	W	Can be read/written only if EFR[4] = 1. These bits are used together with FCTR bits 4-5 to select appropriate trigger level for the transmit FIFO. For detailed information, please refer to the text below this table.
7-6	Rx Trigger Select	W	Can be read/written only if EFR[4] = 1. These bits are used together with FCTR bits 4-5 to select appropriate trigger level for the receive FIFO. For detailed information, please refer to the text below this table.

FCR BIT 4-5:

The FCTR bits 4-5 are associated with these two bits and select one of the 4 tables given below for the transmit trigger level. The IMP16C854 will issue a transmit empty interrupt when the number of characters in the FIFO falls below the selected trigger level.

Table 9 : Transmit Trigger Level Selection Details

FCTR[5:4]	FCR[5:4]	Mode
00 (16C550 Mode)	XX	Trigger level 1. This is the default mode of operation.
01 (16C650 Mode)	00	16
	01	8
	10	24
	11	30
10(16C654 Mode)	00	8
	01	16
	10	32
	11	56
11 (16C850 Mode)	XX	User Programmable trigger level. Programmed in trigger level register.

FCR BIT 6-7: (logic 0 or cleared is the default condition, Rx trigger level = 1)

These bits are used to set the trigger level for the receive FIFO interrupt. The default value that the trigger level takes depends on the FCTR[5:4] and FCR[7:6] bits. After reset, when the FCTR[5:4] are 0's, and the FCR [7:6] are 0's the trigger level is selected as 1.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

Table 10 : Receive Trigger Level Selection Details

FCTR[5:4]	FCR[7:6]	Mode
00 (16C550 Mode)	00	1
	01	4
	10	8
	11	14

Table 10 : Receive Trigger Level Selection Details

FCTR[5:4]	FCR[7:6]	Mode
01 (16C650 Mode)	00	8
	01	16
	10	24
	11	28
10(16C654 Mode)	00	8
	01	16
	10	56
	11	60
11 (16C850 Mode)	XX	User Programmable trigger level. Programmed in trigger level register.

Register Name: **ISR Interrupt Status Register**
Register address: 3'b010.
Post Reset Condition: 0x01.
Register Access Condition: LCR != 0xBF.

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Table 11 : Interrupt Status Register Bits

Bit	Signal	R/W	Description
0	Interrupt Status	R	This bit when high indicates that no interrupt is pending the UART. When low, bits 5-1 indicate the cause of highest priority interrupt pending. For details refer to the table below.
5-1	Highest Interrupt pending	R	When the bit 0 is low, these bits point to the highest priority interrupt pending service in the UART. For details refer to table below.
7-6	FIFO Enable Status	R	These bits are 2'b11 when the FIFO in the UART are enabled. When these bits are read as 2'b00, the UART fifo's are not enabled.

Table 12 : Interrupt Source Table

Priority Level	[ISR BITS]						Source Of The Interrupt	Interrupt clearing
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0		
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)	Read of LSR/ Read of RHR
2	0	0	0	1	0	0	RXRDY (Received Data Ready)	Read of RHR
2	0	0	1	1	0	0	RXRDY (Receive Data Time Out)	Read of RHR
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)	Read of ISR/Write to THR
4	0	0	0	0	0	0	MSR (Modern Status Register)	Read of MSR
5	0	1	0	0	0	0	Received Xoff/Special character.	~~Read of ISR~~ Read of ISR for special charagter interrupt, reception of Xon for Xoff interrupt.
6	1	0	0	0	0	0	CTS/RTS change of state interrupt.	Reset of MSR

Register Name: **LCR -Line Control Register**
Register address: 3'b011.
Post Reset Condition: 0x00.
Register Access Condition: Always Accessible.

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Table 13 : Line control Register Bits

Bit	Signal	R/W	Description
1-0	Character Length	RW	These bits select the bits / character to be transmitted/received. When 00, 5 bits are transmitted and received per character, when 01, 6 bits, when 10, 7 bits and when 11 8 bits are transmitter/received per character. After reset, character length selected is 5 bits.
2	Stop Bits	RW	When 0, one stop bit is transmitter per character.When this bit is set and 5 bits per character is selected as character length, 1.5 stop bits are transmitted per character. When set and any other character length is selected, two stop bits are transmitter per character. Please note that the receiver looks for only one stop bit irrespective of this bit. After reset, the transmitter transmits 1 stop bit per character.
3	Parity Enable	RW	When 0, no parity bit is transmitted or expected by the receiver in the character. When high, a parity bit is transmitted and the receiver expects a parity bit in the character frame.

Table 13 : Line control Register Bits

Bit	Signal	R/W	Description
4	Parity Select	RW	When parity is enabled, this bit when high selects even parity and when low selects odd parity for transmission and reception. For selecting even/odd parity, “Force parity” bit must be 0.
5	Force Parity	RW	When parity is enabled, and this bit is set, parity bit is forced to 1 if “parity select” is set to 0 and parity bit is forced to 0 if “parity select” is set to 1.
6	Transmit Break Enable	RW	When set, the transmitter forces the TX output to logic 0. When cleared, the transmitter starts sending the data from the shift register.
7	DLAB - Divisor Latch Access Bit	RW	When set, enables the baud rate divisor latches to be accessible for programming. When 0, divisor latches are not accessible and THR/RHR and IER register are accessible at the divisor latches addresses.

Register Name: **MCR -Modem Control Register**
Register address: 3’b100.
Post Reset Condition: 0x00.
Register Access Condition: LCR!= 0xBF.

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Table 14 : Modem Control Register Bits

Bit	Signal	R/W	Description
0	DTR Control	RW	When cleared, forces the DTR pin to go high. When set, DTR output is forced low.
1	RTS Control	RW	When cleared, forces the RTS pin to go high. When set, RTS output is forced low.
2	OP1 Control	RW	Bit is used in loopback mode only. This bit is used to control the state of RI interface signal in loopback mode.
3	OP2 Control	RW	When cleared, it forces the INTA-D outputs to tristate operation in intel mode. When set, it forces INTA-D into continuous operation in intel mode. In loopback mode, it is used to control the state of CD.
4	Loopback Mode	RW	When set, it enables loopback mode. When cleared the UART operates in normal mode.
5	Xon Any Enable	RW	Accessible only when the EFR[4]=1. When set, enables special Xon mode in which any Rx character can enable Xon. When cleared, it disables this special flow control mode.
6	Ir Enable	RW	Accessible only when the EFR[4]=1. When set, enables the Ir encoder for transmit data and ir decoder for receive data. When cleared, the TX/RX work in normal mode.

Table 14 : Modem Control Register Bits

Bit	Signal	R/W	Description
7	Clock pre-scaler	RW	Accessible only when the EFR[4]=1. When set, it enables the pre-scaler to provide a divide by 4 clock to the baud rate generator. When cleared, input clock is routed to the baud rate generator.

Register Name: **LSR - Line Status Register**
Register address: 3'b101.
Post Reset Condition: 0x60.
Register Access Condition: LCR!= 0xBF.

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Table 15 : Line Status Register Bits

Bit	Signal	R/W	Description
0	Receive Data Ready	R	When set, it indicates that there is at least 1 received byte in the RHR/RxFifo to be read by the application. It is cleared when there is no data in the RHR/RxFifo. This bit is cleared by the read of RHR/RxFIFO if there is not more data in the RHR/RxFifo.
1	Receive Overrun	R	When set, it indicates that a byte in the receive shift register is lost because the RHR/Rxfifo was full. When clear, it indicates that there is no overrun error. In case an overrun error occurs, the RHR/Rxfifo is not disturbed and the data in the receive shift register is overwritten with the new data. This bit is cleared by read of LSR.
2	Parity Error	R	When set, it indicates that the received byte was detected to have a parity error. It is cleared by a read of RHR/RxFifo. This bit is associated with the data at the top of the FIFO.
3	Framing Error	R	When set, it indicates that the received byte was detected to have a framing error or no stop bit was detected at the end of the character. It is cleared by a read of RHR/RxFifo. This bit is associated with the data at the top of the FIFO.
4	Received Break	R	When set, it indicates that the Rx Input was detected to be in logic 0 state for more than a character time. When this occurs, 1 break byte is transferred to the RxFifo/RHR and this bit is set. It is cleared by a read of RHR/RxFifo. This bit is associated with the data at the top of the FIFO.
5	THR Empty	R	This bit indicates that state of the THR/TxFifo. When set, it indicates that the THR/TxFifo has at least 1 empty location. When cleared, the THR/TxFifo are full.

Table 15 : Line Status Register Bits

Bit	Signal	R/W	Description
6	Transmit Empty	R	This bit when set, indicates that the THR/TxFIFO and the transmit shift register are both empty. When cat logic 0, it indicates that the THR contains at least 1 byte or the TSR is shifting out a data byte.
7	Receive FIFO Error	R	This bit indicates if there is an error associated with the data in the FIFO i.e. at least 1 byte in the RxFifo has either parity error, or framing error or break error. It is cleared when none of the FIFO bytes has a error.

Register Name: **FTR - Factory Test Register**
Register address: 3'b101.
Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF.

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Table 16 : Factory Test Register Bits

Bit	Signal	R/W	Description
0	TxFifoTest Mode	W	When set, it allows direct access to the tx fifo. A write to the Txfifo is done when an access is made to relative address 0 and LCR[7] as 0. No transmit is done in this mode. A read to relative address 0 returns data from the Txfifo. When cleared, device works in normal mode. Cleared by reset or by writing a 0 to the bit.
1	RxFifoTest Mode	W	When set, it allows direct access to the rx fifo. A write to the Rxfifo is done when an access is made to relative address 0 and LCR[7] as 0. A read to relative address 0 returns data from the Rxfifo. When cleared, device works in normal mode. Cleared by reset or by writing a 0 to the bit.
2	Generate Parity Error	W	When set, The transmitter transmits incorrect parity. This enables the design to self test the parity detection and interrupt generation when the tx data is looped back to rx input.
3	Generate Framing Error	W	When set, the transmitter sends stop bit as 0. This enables the design to self test the farming error detection and interrupt generation when the tx data is looped back to rx input externally.
4	Test BRG	W	When set, it enables the test mode for the BRG. In this mode a read access to the DLL/DLM return the counter output. This enables the counter operation to be verified.
7-5	Reserved	-	Reserved. Must be written as 0.

Register Name: **MSR - Modem Status Register**
Register address: 3'b110.
Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF.

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Table 17 : Modem Status Register Bits

Bit	Signal	R/W	Description
0	Delta CTS	R	When set, it indicates that there was a change in the state of the CTS since the last read of the MSR. It is cleared when the MSR is read.
1	Delta DSR	R	When set, it indicates that there was a change in the state of the DSR since the last read of the MSR. It is cleared when the MSR is read.
2	Delta RI	R	When set, it indicates that RI input changed from logic 0 to logic 1 since the last read of the MSR. It is cleared when the MSR is read
3	Delta CD	R	When set, it indicates that there was a change in the state of the CD since the last read of the MSR. It is cleared when the MSR is read.
4	CTS Input Status	R	This bit indicates the inverted state of the CTS input. In loopback mode, it indicates the state of RTS bit in the MCR.
5	DSR Input Status	R	This bit indicates the inverted state of the DSR input. In loop-back mode, it indicates the state of DTR bit in the MCR.
6	RI Input Status	R	This bit indicates the inverted state of the RI input. In loopback mode, it indicates the state of OP1 bit in the MCR.
7	CD Input State	R	This bit indicates the inverted state of the CD input. In loopback mode, it indicates the state of OP2 bit in the MCR.

Register Name: **SPR - Scratch Pad Register**
Register address: 3'b111.
Post Reset Condition: 0xFF.
Register Access Condition: LCR != 0xBF & FCTR[6] = 0.

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Table 18 : SP Register Bits

Bit	Signal	R/W	Description
7-0	Scratch Pad Data	RW	General purpose byte store register.

Register Name: **FLVLR - Fifo Level Register**
Register address: 3'b111.

Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF & FCTR[6] = 1.

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Table 19 : FLVL Register Bits

Bit	Signal	R/W	Description
7-0	Fifo Levels	R	This register indicates the number of bytes in the RxFifo/TxFifo. When EMSR[0] is logic 0, a read of this register returns the RxFifo level, while when the EMSR[0] is 1, it returns the TxFifo Level. Please refer to description of EMSR[1:0] bits for further details.

Register Name: **EMSR - Enhanced Mode Select Register**
Register address: 3'b111.
Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF & FCTR[6] = 1.

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Table 20 : EMS Register Bits

Bit	Signal	R/W	Description
1-0	Fifo Count	W	When EMSR[0] is 0, a read of FLVL register returns the RxFifo byte count. When these bits are 2'b01, the TxFIFO byte count is returned with a read of the FLVL Register. When these bits are 2'b11, the Rx and Tx FIFO byte counts are returned with alternate reads of the FLVL register. After these bits are set to 2'b11, the first read of the FLVL register returns the RxFifo byte count.
3-2	Reserved	-	Write 0's to these bits.
5-4	RTS Hysteresis	W	These bits select the RTS flow control hysteresis. These bits are valid only when FCTR[5:4] are 2'b11. These bits determine when the RTS output is set/cleared with auto out-of-band flow control and user selectable trigger levels are selected. For details refer to table below.
7-6	Reserved	-	Writes 0's to these bits.

The following table provides details of RTS hysteresis.

Table 21 : RTS Hysteresis

FMSR[5:4]	FCTR[1:0]	RTS Hysteresis
00	00	Next Level (Default)
	01	+/-4 Characters
	10	+/-6 Characters
	11	+/-8 Characters
01	00	+/-8 Characters
	01	+/-16 Characters
	10	+/-24 Characters
	11	+/-32 Characters
10	00	+/-12 Characters
	01	+/-20 Characters
	10	+/-28 Characters
	11	+/-36 Characters
11	00	+/-40 Characters
	01	+/-44 Characters
	10	+/-48 Characters
	11	+/-52 Characters

Register Name: **DLL - Divisor Latch LSB Register**
Register address: 3'b000.
Post Reset Condition: 0x00.
Register Access Condition: LCR != 0xBF & LCR[7] = 1.

Table 22 : DLL Register Bits

Bit	Signal	R/W	Description
7-0	Divisor Count - lower Byte	RW	This 8 bit value is the lower byte of the clock divisor used to generate the baud rate.

Register Name: **DLM - Divisor Latch MSB Register**
Register address: 3'b001.
Post Reset Condition: 0x00.

Register Access Condition: LCR!= 0xBF & LCR[7] = 1.

Table 23 : DLM Register Bits

Bit	Signal	R/W	Description
7-0	Divisor Count - Upper Byte	RW	This 8 bit value is the higher byte of the clock divisor used to generate the baud rate.

Register Name: **TRG - Trigger Level Register**
Register address: 3'b000.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 24 : TRG Register Bits

Bit	Signal	R/W	Description
7-0	Trigger Level/ FIFO Level	RW	This register allows the user to program the trigger level for the receive and transmit FIFO's. When FCTR[7] = 0, a write to this register will allow setting the receive FIFO trigger level. A read of this register returns the number of bytes in the receive FIFO. When FCTR[7]=1, a write to this register will allow setting the transmit trigger level. A read of this register returns the number of bytes in the transmit FIFO.

Register Name: **FCTR - Feature Control Register**
Register address: 3'b001.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 25 : FCTR Register Bits

Bit	Signal	R/W	Description
1-0	RTS Hysteresis Level Select	RW	Control the RTS Delay Trigger levels for the FIFO. For more details refer to the description of the EMSR Register.
2	Rx Input Select	RW	When 0, the Rx Input is assumed to be encoded IrDA data. When 1, Rx input is assumed to be active high encoded IrDA data.
3	Auto RS485 Enable	RW	When enabled (this bit is set), the THR empty interrupt generation condition is changed from THR empty to TSR empty.
5-4	Tx/Rx Fifo Trigger level Table Select	RW	Allows selection of the TX/Rx trigger table. Please refer to FCR description for more details.
6	SPR Swap	RW	Control selection of SPR/FLVL & EMSR registers at address 3'b111. When set, it allows the application to access the FLVL/ EMSR registers. When at logic 0, it allows access to SPR for the application.

Table 25 : FCTR Register Bits

Bit	Signal	R/W	Description
7	Rx/Tx Mode	RW	Allows the application to set the user programmable trigger levels for Rx/Tx fifo in the TRG register. For details refer to TRG register description.

Register Name: **EFR - Enhanced Feature Register**
Register address: 3'b010.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 26 : EFR Register Bits

Bit	Signal	R/W	Description
3-0	In Band Flow Control	RW	These bits control the operation of the device for in-band flow control. Please refer to table below for more details.
4	Enhanced Function Bits Enable	RW	This bit when set, enables the programming/ control of enhanced features described in IER[7:4], ISR[5:4], FCR[5:4], MCR[7:5] bits. In order to program these bits, the EFR[4] needs to be 0. The bits can be programmed and then when a 0-1 transition is made on this bit, these features are enabled.
5	Special Character Detect Enable	RW	When enabled (this bit is set), any incoming character is compared with the byte programmed in Xoff2 and if a match exists, the data is transferred to FIFO and ISR bit 4 is set. When this feature is enabled, in-band flow control should be disabled.
6	Auto RTS Flow Control Enable	RW	When set, it allows the RTS to control the data flow. When cleared, RTS acts as a general purpose output. When RTS flow control is enabled, the RTS output is automatically deasserted when the receive fifo level reaches the next upper level to the trigger level selected or programmed RTS hysteresis level is reached. It is asserted again when the receive FIFO level reaches the next lower trigger level to the trigger level selected. This allows some hysteresis and smoother flow control.
7	Auto CTS flow Control	RW	When set, it allows the CTS to control the transmitter data flow. When cleared, CTS acts as a general purpose input. when enabled, the CTS controls the transmitter. When the inputs is asserted, the transmitter transmits data. When the input is deasserted, the transmitter stops transmitting data after completion of transmission of current character. It resumes transmission after the CTS is asserted.

The following table describes the functionality of the EFR[3:0].

Table 27 : In-band flow control Details

EFR[3:0]	In band Flow Control Function
00xx	No Transmit Flow Control. i.e. receiver FIFO condition cannot force the transmitter to transmit in-band flow control characters.
10xx	Transmit Xon1/Xoff1 for in-band flow control - The transmitter transmits the Xoff1 character as soon as the selected receive FIFO trigger level +2 is reached. It sends the Xon1 character when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth.
01xx	Transmit Xon2/Xoff2 for in-band flow control - The transmitter transmits the Xoff2 character as soon as the selected receive FIFO trigger level is reached +2. It sends the Xon2 character when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth.
11xx	Transmit Xon1,Xon2/Xoff1,Xoff2 for in-band flow control -The transmitter transmits theXoff1 and Xoff2 characters in that sequence as soon as the selected receive FIFO trigger level+2 is reached. It sends the Xon1 and Xon2 character in that sequence when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth.
xx00	No Rx Flow control. Receiver does not compare incoming characters with programmed flow control characters to control the transmitter operation.
xx10	Receiver Compares Xon1/Xoff1 - The receiver compares the incoming characters with the Xoff1 character and disables the transmitter of that channel from the following byte. The receiver continues to monitor the incoming receive stream and when it finds the comparison to Xon1 matches, it enables the transmitter to resume the transmission.
xx01	Receiver Compares Xon2/Xoff2. The receiver compares the incoming characters with the Xoff2 character and disables the transmitter of that channel from the following byte. The receiver continues to monitor the incoming receive stream and when it finds the comparison to Xon2 matches, it enables the transmit to resume the transmission.
0011	Receiver Compares Xon1,Xon2/Xoff1,Xoff2. No transmit flow control. The receiver compares the incoming characters with the Xoff1 and Xoff2 character in the incoming data stream in that sequence and disables the transmitter of that channel from the following byte. The receiver continues to monitor the incoming receive stream and when it finds the comparison to Xon1 and Xon2 matches for two sequential incoming data bytes, it enables the transmitter to resume the transmission. There is not flow control exercised for the receive FIFO and the transmitter does not transmit flow control characters.
1111	Receiver Compares Xon1,Xon2/Xoff1,Xoff2. Transmit Xon1,Xon2/Xoff1,Xoff2 for in-band flow control. The receiver compares the incoming characters with the Xoff1 and Xoff2 character in the incoming data stream in that sequence and disables the transmitter of that channel from the following byte. The receiver continues to monitor the incoming receive stream and when it finds the comparison to Xon1 and Xon2 matches for two sequential incoming data bytes, it enables the transmitter to resume the transmission. The transmitter transmits theXoff1 and Xoff2 characters in that sequence as soon as the selected receive FIFO trigger level +2 is reached. It sends the Xon1 and Xon2 character in that sequence when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth

Table 27 : In-band flow control Details

EFR[3:0]	In band Flow Control Function
1011	Transmit Xon1/Xoff1 for in-band flow control. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2. The transmitter transmits the Xoff1 character as soon as the selected receive FIFO trigger level +2 is reached. It sends the Xon1 character when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth. The receiver compares the incoming character with both Xoff1 and Xoff2 and if the incoming character matches with any one of the two characters, the transmitter is disabled following the completion of transmission of current character. The receiver continues to monitor the incoming receive data stream and when it finds that a Xon1 or Xon2 character is received, it enables the transmitter to resume transmission.
0111	Transmit Xon2/Xoff2 for in-band flow control. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2. The transmitter transmits the Xoff2 character as soon as the selected receive FIFO trigger level +2 is reached. It sends the Xon2 character when the receive fifo level reaches the a level that is immediately lower to selected Rx Fifo trigger level or programmed RTS hysteresis level because of removal of characters from the receive fifo by the application. This provides a hysteresis and the flow control characters do not consume a lot of available serial data bandwidth. The receiver compares the incoming character with both Xoff1 and Xoff2 and if the incoming character matches with any one of the two characters, the transmitter is disabled following the completion of transmission of current character. The receiver continues to monitor the incoming receive data stream and when it finds that a Xon1 or Xon2 character is received, it enables the transmitter to resume transmission.

Register Name:**Xon1 Register**
Register address: 3'b100.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 28 : Xon1 Register Bits

Bit	Signal	R/W	Description
7-0	Xon1 Byte	RW	This is the 8 bit Xon1 byte. Number of bits used from this register for transmission/receive compare function depends on the LCR[1:0].

Register Name:**Xon2 Register**
Register address: 3'b101.
Post Reset Condition: 0x00
Register Access Condition: LCR = 0xBF.

Table 29 : Xon2 Register Bits

Bit	Signal	R/W	Description
7-0	Xon2 Byte	RW	This is the 8 bit Xon2 byte. Number of bits used from this register for transmission/receive compare function depends on the LCR[1:0].

Register Name:**Xoff1 Register**
Register address: 3'b110.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 30 : Xoff1 Register Bits

Bit	Signal	R/W	Description
7-0	Xoff1 Byte	RW	This is the 8 bit Xoff1 byte. Number of bits used from this register for transmission/receive compare function depends on the LCR[1:0].

Register Name:**Xoff2 Register**
Register address: 3'b111.
Post Reset Condition: 0x00.
Register Access Condition: LCR = 0xBF.

Table 31 : Xoff2 Register Bits

Bit	Signal	R/W	Description
7-0	Xoff2 Byte	RW	This is the 8 bit Xoff2 byte. Number of bits used from this register for transmission/receive compare function depends on the LCR[1:0]. This byte is also used while comparing for special receive character.

Register Name: **FIFO Status Register**
Register address: FSRS should be low. Accessed only in QPF100 package.
Post Reset Condition: 0x00.
Register Access Condition: None.

Table 32 : FSTAT Register Bits

Bit	Signal	R/W	Description
0	TXRDYA	R	This bit indicates status of TXRDY of channel A. When DMA mode 0 is selected in the FCR, this bit is logic 0 when TxFIFO is not empty.When 1 it indicates TXFIFO completely empty. When DMA mode 1 is selected, this bit is 0 with the TxFIFO is full and 1 when TxFIFO is not full.
1	TXRDYB	R	This bit indicates status of TXRDY of channel B. When DMA mode 0 is selected in the FCR, this bit is logic 0 when TxFIFO is not empty.When 1 it indicates TXFIFO completely empty. When DMA mode 1 is selected, this bit is 0 with the TxFIFO is full and 1 when TxFIFO is not full.

Table 32 : FSTAT Register Bits

Bit	Signal	R/W	Description
2	TXRDYC	R	This bit indicates status of TXRDY of channel C. When DMA mode 0 is selected in the FCR, this bit is logic 0 when TxFIFO is not empty.When 1 it indicates TXFIFO completely empty. When DMA mode 1 is selected, this bit is 0 with the TxFIFO is full and 1 when TxFIFO is not full.
3	TXRDYD	R	This bit indicates status of TXRDY of channel D. When DMA mode 0 is selected in the FCR, this bit is logic 0 when TxFIFO is not empty.When 1 it indicates TXFIFO completely empty. When DMA mode 1 is selected, this bit is 0 with the TxFIFO is full and 1 when TxFIFO is not full.
4	RxRDYA	R	When DMA mode 0 is selected, this bit is low when RxFIFO is empty and 1 when RxFIFO is not empty. When DMA mode 1 is selected, this bit is low when receive FIFO has not reached the trigger level. It is high when the programmed trigger level is reached or receive time-out has occurred.
5	RxRDYB	R	When DMA mode 0 is selected, this bit is low when RxFIFO is empty and 1 when RxFIFO is not empty. When DMA mode 1 is selected, this bit is low when receive FIFO has not reached the trigger level. It is high when the programmed trigger level is reached or receive time-out has occurred.
6	RxRDYC	R	When DMA mode 0 is selected, this bit is low when RxFIFO is empty and 1 when RxFIFO is not empty. When DMA mode 1 is selected, this bit is low when receive FIFO has not reached the trigger level. It is high when the programmed trigger level is reached or receive time-out has occurred.
7	RxRDYD	R	When DMA mode 0 is selected, this bit is low when RxFIFO is empty and 1 when RxFIFO is not empty. When DMA mode 1 is selected, this bit is low when receive FIFO has not reached the trigger level. It is high when the programmed trigger level is reached or receive time-out has occurred.

AC Electrical Characersitics

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 -V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Units	Conditions
		Min	Max		
T_{1w},T_{2w}	Clock pulse duration	20		ns	
T_{3w}	Oscillator /Clock frequency		24	MHz	
T_{6s}	Address setup time	10		ns	

Symbol	Parameter	Limits 3.3		Units	Conditions
		Min	Max		
T_{7w}	$\overline{IOR}$ strobe width	35		ns	
T_{7d}	$\overline{IOR}$ Delay from $\overline{CS}$	10		ns	
T_{7h}	Address hold time	10		ns	
T_{9d}	Read cycle delay	40		ns	
T_{12d}	Delay from $\overline{IOR}$ to data		35	ns	
T_{12h}	Data disable time		25	ns	
T_{13d}	$\overline{IOW}$ Delay from $\overline{CS}$	10		ns	
T_{13w}	$\overline{IOW}$ strobe width	35		ns	
T_{13h}	Address hold time from $\overline{IOW}$	10		ns	
T_{15d}	write cycle delay	40		ns	
T_{16s}	Data setup time	10		ns	
T_{16h}	Data hold time	10		ns	
T_{17d}	Delay from $\overline{IOW}$ to output		50	ns	100pF load
T_{18d}	Delay to set interrupt from MODEM input		40	ns	100pF load
T_{19d}	Delay to reset interrupt from $\overline{IOR}$		40	ns	100pF load
T_{20d}	Delay from stop to set interrupt		1	RCLK	
T_{21d}	Delay from $\overline{IOR}$ to reset interrupt		40	ns	100pF load
T_{22d}	Delay from start to interrupt		100	ns	
T_{22drs}	Delay from stop to interrupt		45	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	RCLK	
T_{24d}	Delay from $\overline{IOW}$ to reset interrupt		45	ns	
T_{25d}	Delay from stop to set $\overline{RxRdy}$		1	RCLK	
T_{26d}	Delay from $\overline{IOR}$ to reset $\overline{RxRdy}$		45	ns	
T_{27d}	Delay from $\overline{IOW}$ to set $\overline{TxRdy}$		45	ns	
T_{28d}	Delay from start to reset $\overline{TxRdy}$		8	RCLK	
T_{30s}	Address setup time	10		ns	
T_{30w}	Chip select strobe width	40		ns	

Symbol	Parameter	Limits 3.3		Units	Conditions
		Min	Max		
T_{30s}	Address hold time	15		ns	
T_{30d}	Read cycle delay	70		ns	
T_{31d}	Delay from $\overline{CS}$ to data		15	ns	
T_{31h}	Data disable time	4	15	ns	
T_{32s}	RWn strobe setup time	10		ns	
T_{32h}	RWn strobe hold time	10		ns	
T_{32d}	Write cycle delay	70		ns	
T_{33s}	Data setup time	20		ns	
T_{33h}	Data hold time	10		ns	
T_R	Reset pulse width	40		ns	
N	Baud rate divisor	1	2^{16}-1	RCLK	

Absolute Maximum Ratings

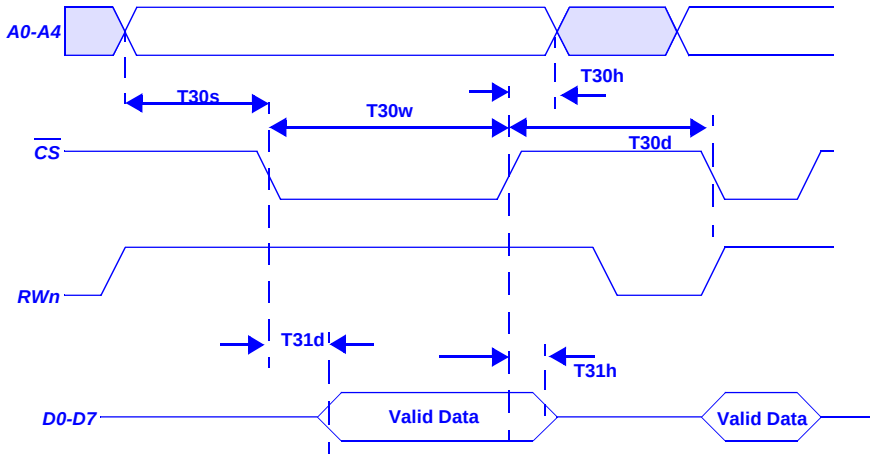
Supply range	4 Volts (to be confirmed)
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Package dissipation	????? mW
Stand-by-current	????? mA.

DC Electrical Characteristics

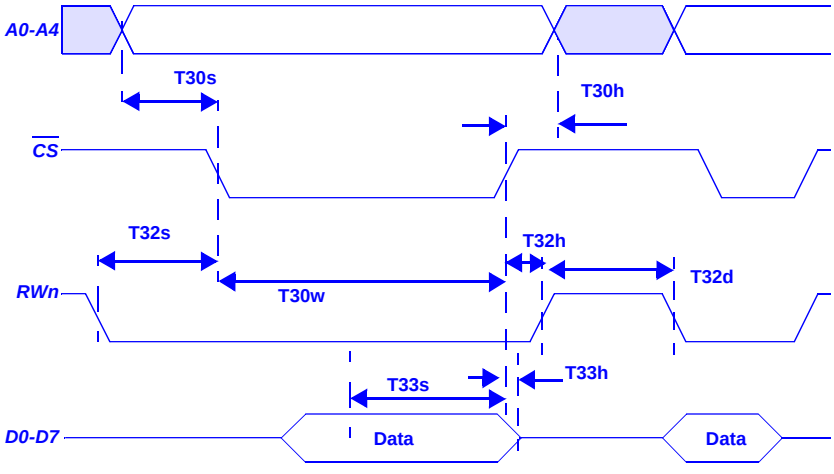
T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Units	Conditions
		Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	V	
V_{IHCK}	Clock input high level	2.4	VCC	V	
V_{IL}	Input low level	-0.3	0.8	V	

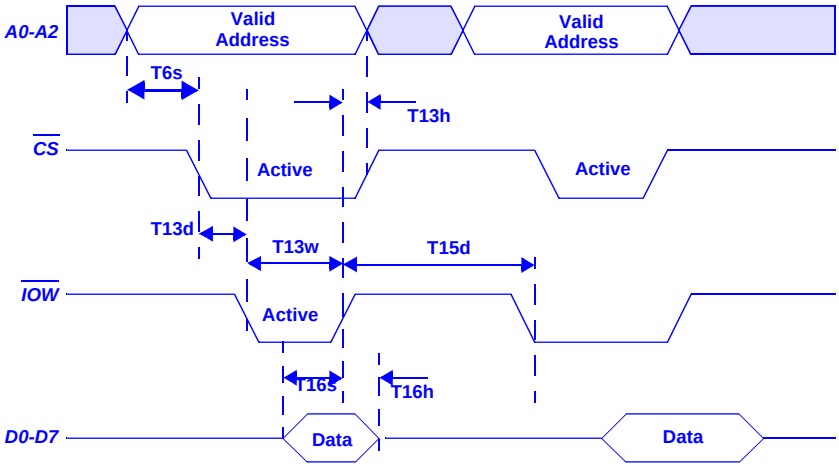
Symbol	Parameter	Limits 3.3		Units	Conditions
		Min	Max		
V_{IH}	Input high level	2.0	VCC	V	
V_{OL}	Output low level on all outputs		O.4	V	I_{OL} = 4 mA
V_{OH}	Output high level	2.0		V	I_{OH} = -1 mA
I_{IL}	Input leakage		± 10	µA	
I_{CL}	Clock leakage		± 10	µA	
I_{CC}	Avg power supply current		3	mA	
C_P	Input capacitance		5	pF	
R_{IN}	Internal pull-up resistance	40	80	kohms	



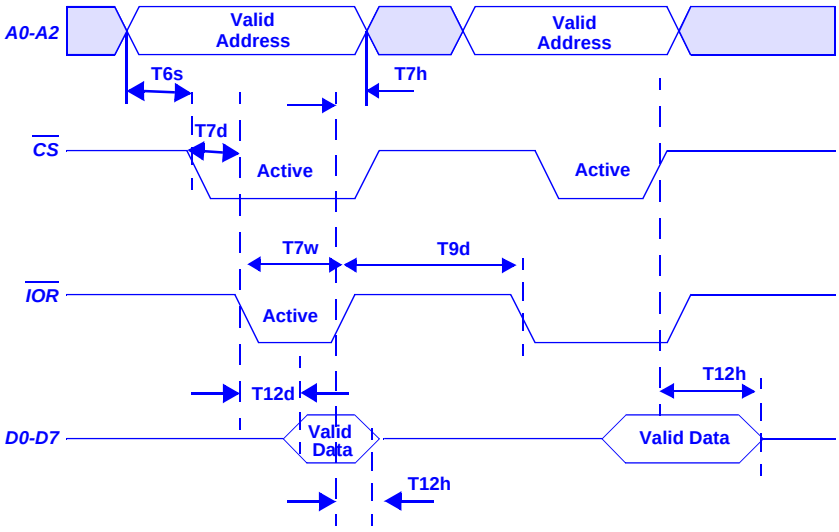
General read Timing In Motorola Mode



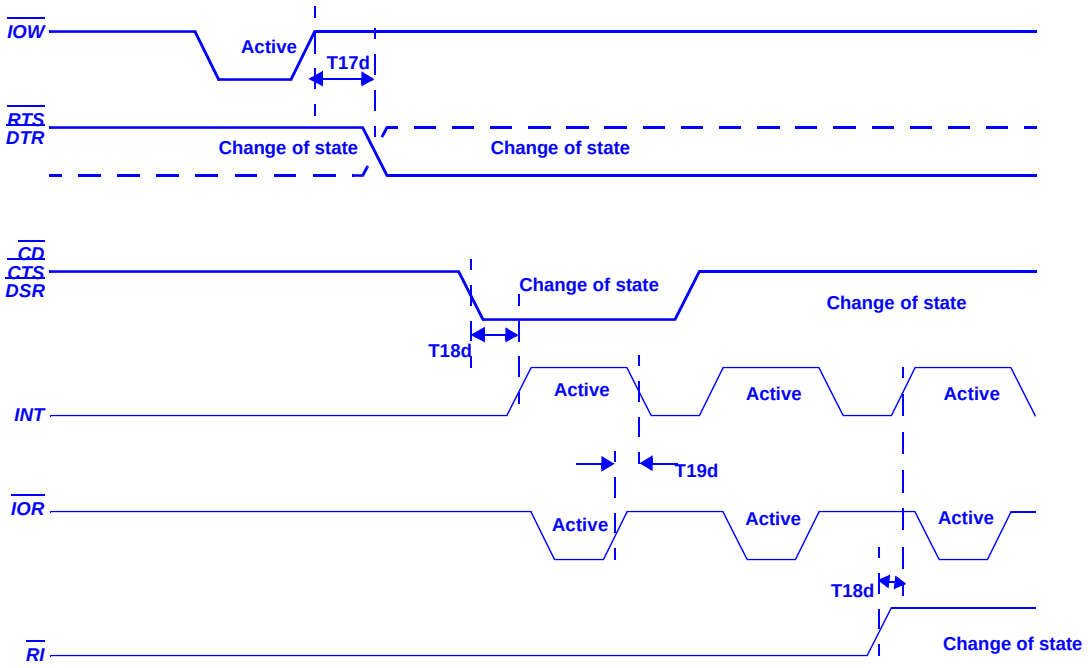
General Write Timing In Motorola Mode



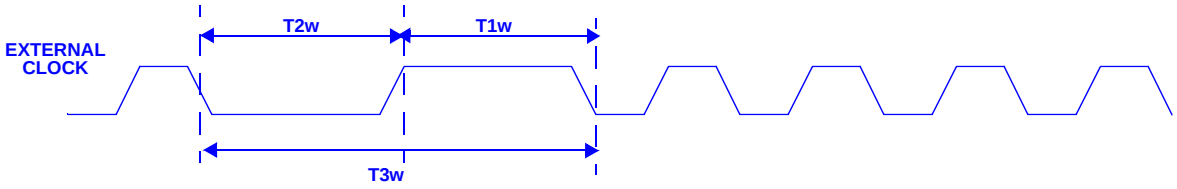
General Write Timing In Intel Mode



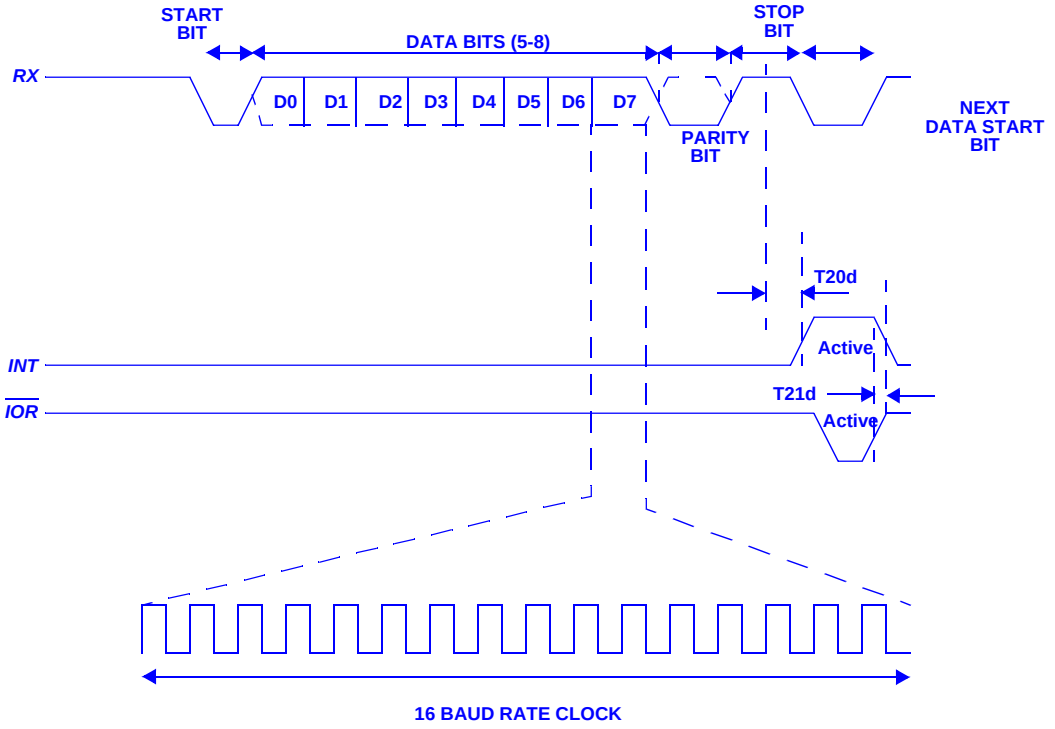
General read timing in Intel mode



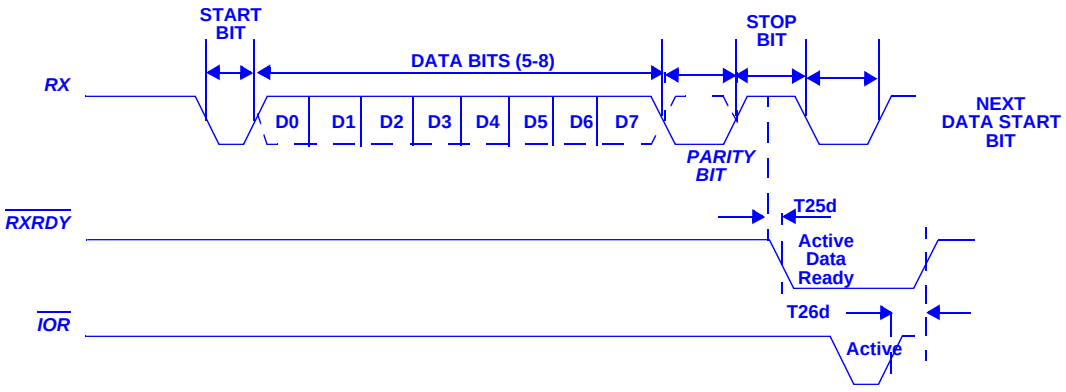
Modem Input/output Timing



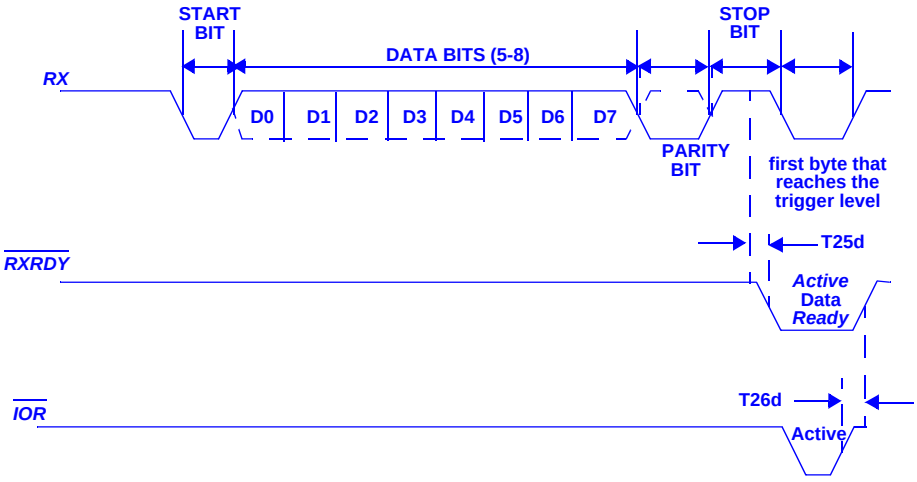
External Clock Timing



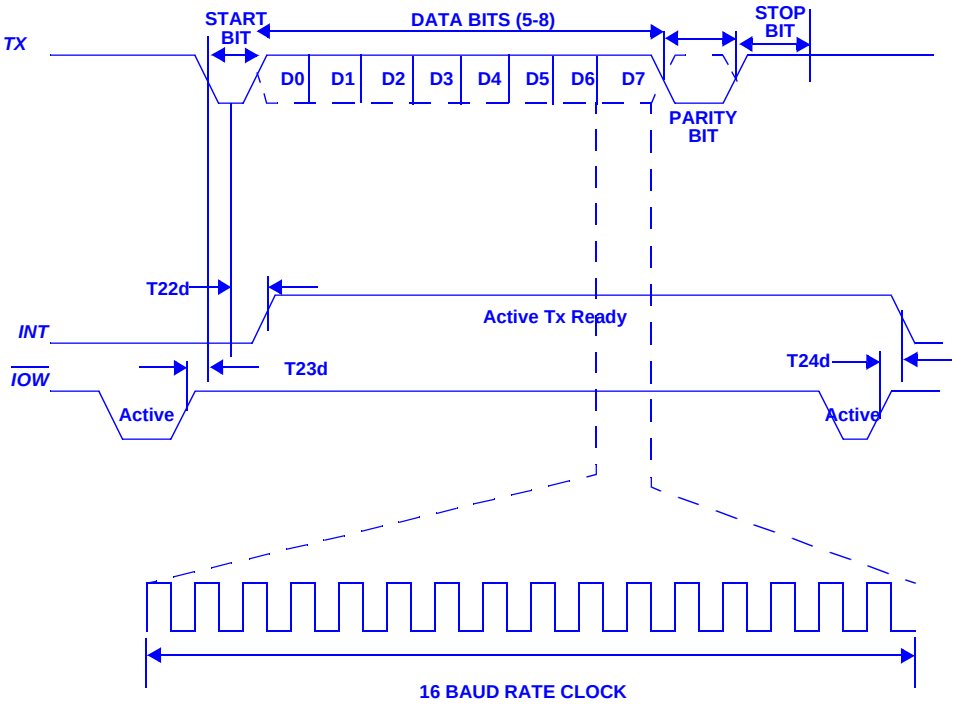
Receive Timing



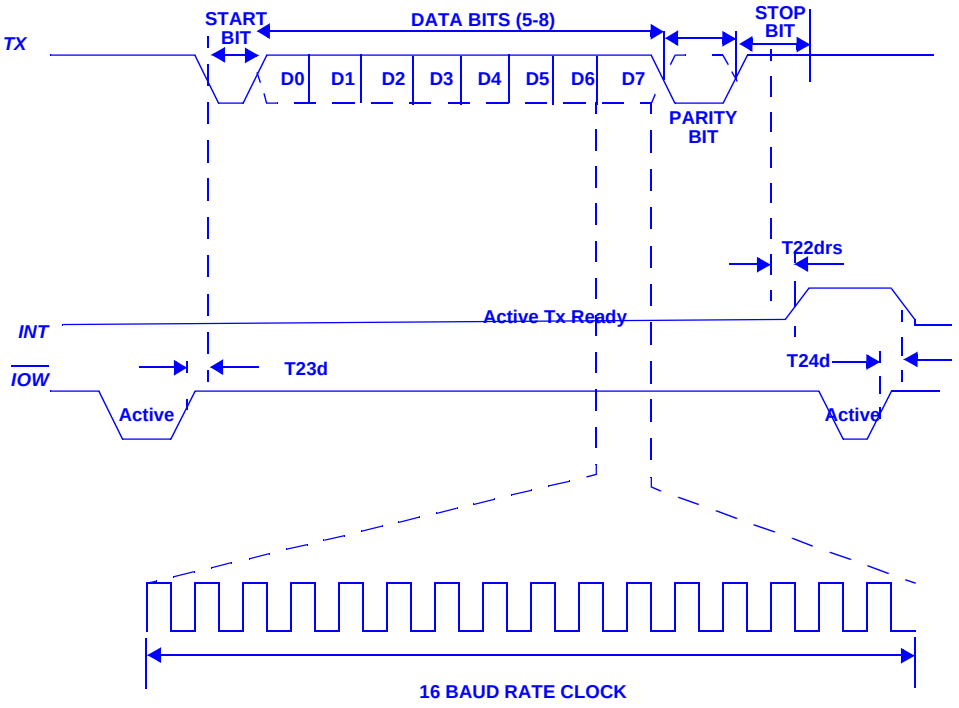
Receive ready timing in non FIFO mode



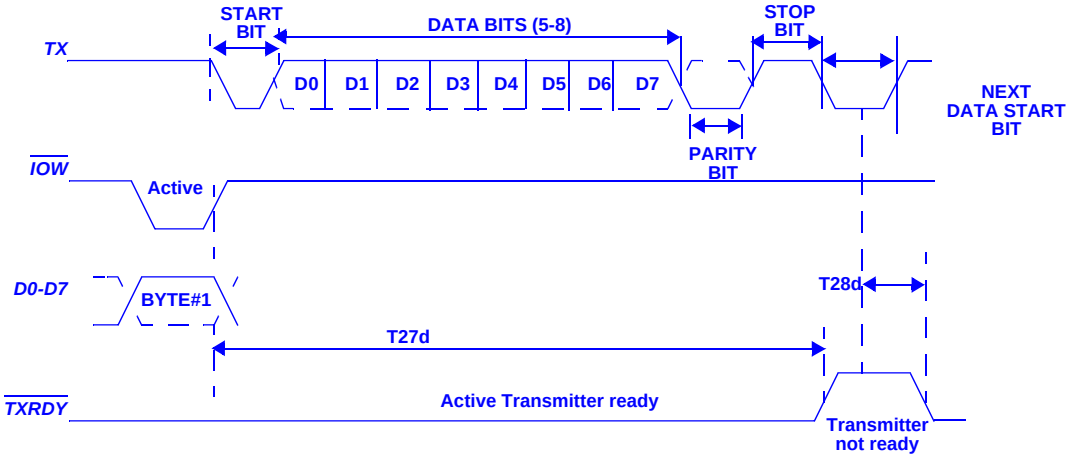
Receive timing in FIFO mode



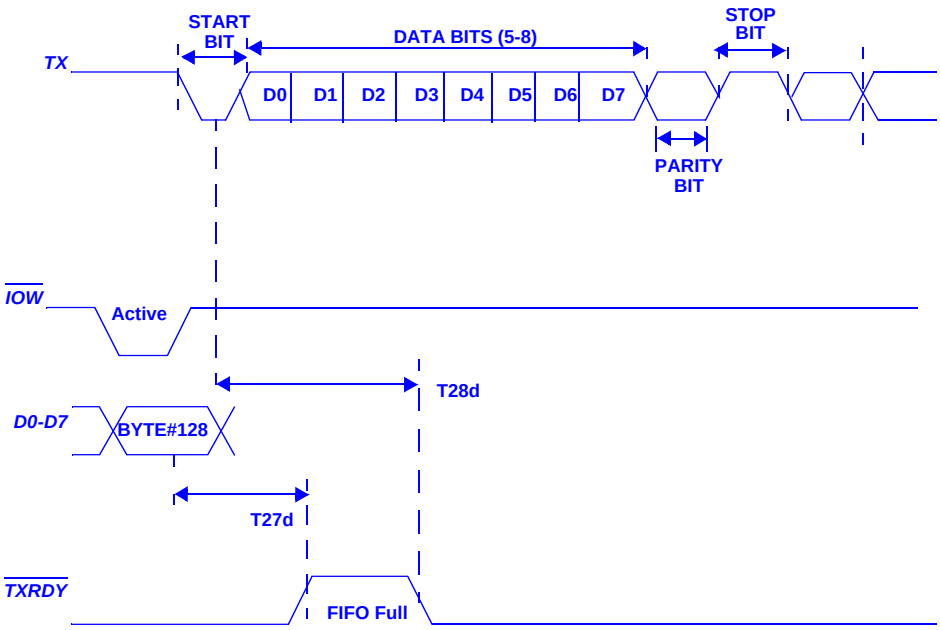
Transmit Timing in normal mode



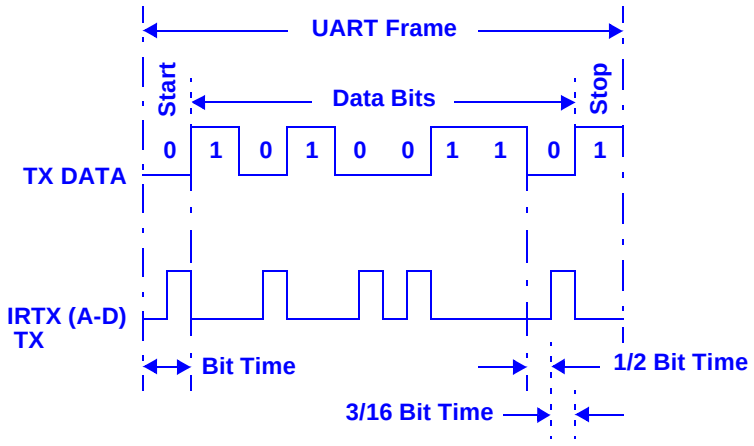
Transmit Timing in RS485 mode



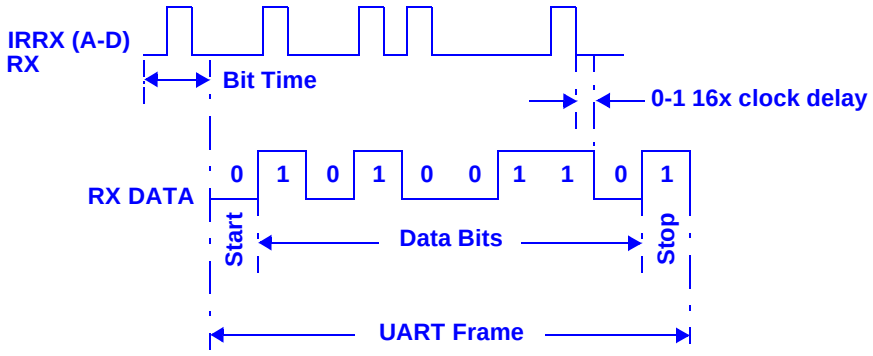
Transmit ready timing in non-FIFO mode



Transmit ready timing in FIFO mode



Infrared Transmit Timing



Infrared Receive Timing

ISO 9001 Registered

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