Low-Power µP Supervisor Circuits

- Watchdog timer
- Brownout detection
- Power supply monitor

The IMP705/706/707/708 and IMP813L CMOS supervisor circuits monitor power-supply and battery voltage level, and µP/µC operation. Compared to pin-compatible devices offered by Maxim Integrated Products, IMP devices feature 60 percent lower maximum supply current.

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions. A reset is generated when the supply drops below 4.65V (IMP705/707/813L) or 4.40V (IMP706/708). For 3V power supply applications, refer to the IMP705P/R/S/T data sheet. In addition, the IMP705/706/813L feature a 1.6 second watchdog timer. The IMP707/708 have both active-HIGH and active-LOW reset outputs but no watchdog function. The IMP813L has the same pin-out and functions as the IMP705 but has an active-HIGH reset output. A versatile power-fail circuit has a 1.25V threshold, useful in checking battery levels and non-5V supplies. All devices have a manual reset ($\overline{MR}$) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in 8-pin DIP, SO and MicroSO packages.

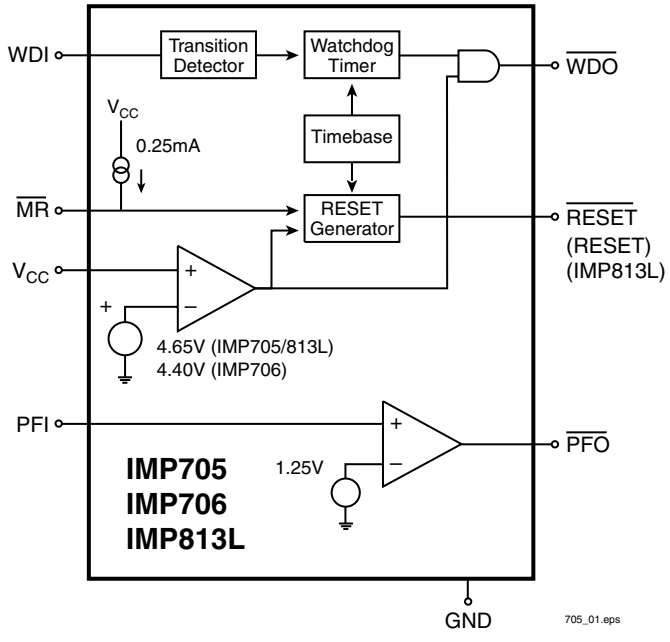
Key Features

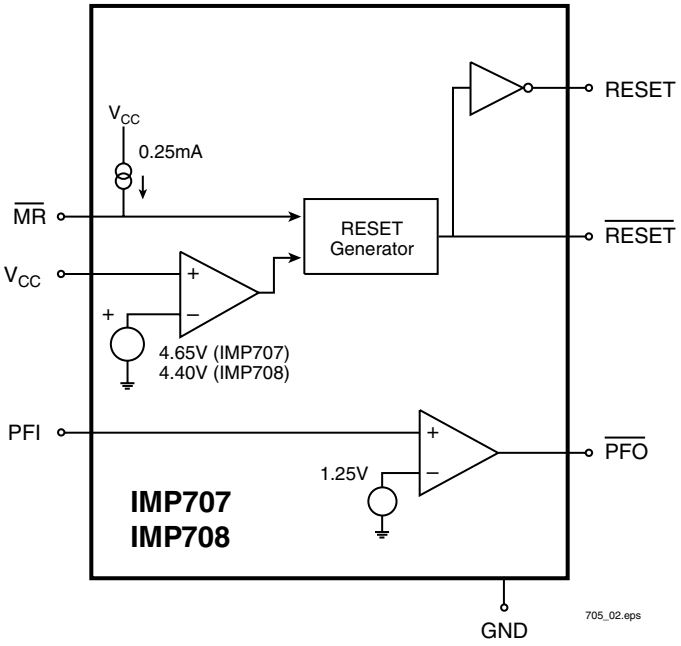
- Improved replacements for the Maxim MAX705/6/7/8, MAX813L
  - 140µA maximum supply current
  - 60% improvement
- Precision power supply monitor
  - 4.65V threshold (IMP705/707/813L)
  - 4.40V threshold (IMP706/8)
- Debounced manual reset input
- Voltage monitor
  - 1.25V threshold
  - Battery monitor/Auxiliary supply monitor
- Watchdog timer (IMP705/706/813L)
- 200ms reset pulse width
- Active HIGH reset output (IMP707/708/813L)
- MicroSO package

Applications

- Computers and embedded controllers
- Battery-operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

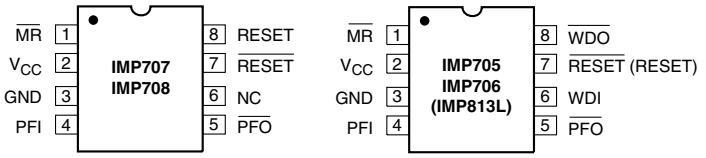
Block Diagrams



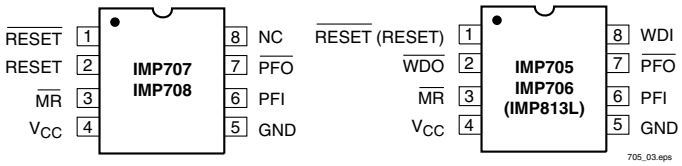


Pin Configuration

DIP/SO



MicroSO



Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
IMP705 Active LOW Reset, Watchdog Output and Manual RESET			
IMP705CPA	4.65	0°C to +70°C	8-Plastic DIP
IMP705CSA	4.65	0°C to +70°C	8-SO
IMP705CUA	4.65	0°C to +70°C	8-MicroSO
IMP705C/D	4.65	25°C	Dice
IMP705EPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP705ESA	4.65	–40°C to +85°C	8-SO
IMP706ESA	4.40	–40°C to +85°C	8-SO
IMP706 Active LOW Reset, Watchdog Output and Manual RESET			
IMP706CPA	4.40	0°C to +70°C	8-Plastic DIP
IMP706CSA	4.40	0°C to +70°C	8-SO
IMP706CUA	4.40	0°C to +70°C	8-MicroSO
IMP706C/D	4.40	25°C	Dice
IMP706EPA	4.40	–40°C to +85°C	8-Plastic DIP
IMP706ESA	4.40	–40°C to +85°C	8-SO
IMP707 Active LOW & HIGH Reset with Manual RESET			
IMP707CPA	4.65	0°C to +70°C	8-Plastic DIP
IMP707CSA	4.65	0°C to +70°C	8-SO
IMP707CUA	4.65	0°C to +70°C	8-MicroSO
IMP707C/D	4.65	25°C	Dice
IMP707EPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP707ESA	4.65	–40°C to +85°C	8-SO
IMP708 Active LOW & HIGH Reset with Manual RESET			
IMP708CPA	4.40	0°C to +70°C	8-Plastic DIP
IMP708CSA	4.40	0°C to +70°C	8-SO
IMP708CUA	4.40	0°C to +70°C	8-MicroSO
IMP708C/D	4.40	25°C	Dice
IMP708EPA	4.40	–40°C to +85°C	8-Plastic DIP
IMP708ESA	4.40	–40°C to +85°C	8-SO
IMP813L Active HIGH Reset, Watchdog Output and Manual RESET			
IMP813LCPA	4.65	0°C to +70°C	8-Plastic DIP
IMP813LCSA	4.65	0°C to +70°C	8-SO
IMP813LCUA	4.65	0°C to +70°C	8-MicroSO
IMP813LC/D	4.65	25°C	Dice
IMP813LEPA	4.65	–40°C to +85°C	8-Plastic DIP
IMP813LESA	4.65	–40°C to +85°C	8-SO

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground
V_{CC} . . . . . -0.3V to 6.0V
All other inputs[1] . . . . . -0.3V to (V_{CC}+0.3V)
Input Current at V_{CC} and GND 20mA
Output Current: All outputs 20mA
Rate of Rise at V_{CC} 100V/µs
Plastic DIP Power Dissipation . . . . . 700 mW
(Derate 9 mW/°C above 70°C)
SO Power Dissipation . . . . . 470 mW
(Derate 5.9 mW/°C above 70°C)
MicroSO Power Dissipation 330mW
(Derate 4.1 mW/°C above 70°C)

Operating Temperature Range
IMP705E/706E/707E/708E/813LE . . . . . –40°C to 85°C
IMP706C/707C/708C/813LC . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to 160°C
Lead Temperature Soldering(10 sec) . . . . . 300°C

Note: 1. The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

These are stress ratings only and functional operation is not implied.

Electrical Characteristics

Typical values at Ta=25°C, V_{CC} = 5V to 5.5V for the IMP705C/E,707C/E,813L.
V_{CC}= 5V to 5.5V for the IMP706C/E,708C/E.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage Range	V_{CC}	IMP705/6/7/8C	1.2		5.5	V
		IMP813L	1.1		5.5	
		IMP705/6/7/8E, IMP813lE	1.2		5.5	
Supply Current	I_{CC}	IMP705C/706C/813LC		75	140	µA
		IMP705E, IMP706E, IMP813LE		75	140	
		IMP707C, IMP708C		50	140	
		IMP707E, IMP708E		50	140	
RESET Threshold	V_{RT}	IMP705, IMP707, IMP813L, Note 2	4.50	4.65	4.75	V
		IMP706, IMP708, Note 2	4.25	4.40	4.50	
RESET Threshold Hysteresis		Note 2		40		mV
RESET Pulse Width	t_{RS}	Note 2	140	200	280	ms
$\overline{MR}$ Pulse Width	t_{MR}		0.15			µs
$\overline{MR}$ to RESET Out Delay	t_{MD}	Note 2			0.25	µs
$\overline{MR}$ Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
$\overline{MR}$ Pull-up Current		$\overline{MR}$ = 0V	100	250	600	µA
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	Vcc-1.5V			V
		I_{SINK} = 3.2mA			0.4	
		IMP705/6/7/8, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		IMP707/708/813L, I_{SOURCE} = 800µA	Vcc-1.5V			V
		IMP707/708, I_{SINK} = 1.2mA			0.4	
		IMP813L, I_{SINK}= 3.2mA			0.4	
		IMP813L, V_{CC} =1.2V, I_{SOURCE} = 4µA				
Watchdog Timeout Period	t_{WD}	IMP705/706/813L	1.00	1.60	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold	V_{IH}	IMP705/706/813L, V_{CC} = 5V	3.5			V
	V_{IL}				0.8	
WDI Input Current		IMP705/706/813L, WDI = V_{CC}		50	150	µA
		IMP705/706/813L, WDI = 0V	–150	–50		
$\overline{WDO}$ Output Voltage		IMP705/706/813L, I_{SOURCE} = 800µA	Vcc-1.5V			V
		IMP705/706/813L, I_{SINK} = 1.2mA			0.4	
PFI Input Threshold		V_{CC} = 5V	1.2	1.25	1.3	V
PFI Input Current			–25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA	Vcc - 1.5V			V
		I_{SINK} = 3.2mA			0.4	

Notes: 2. $\overline{RESET}$ (IMP705/6/7/8), RESET (IMP707/8, IMP813L)

Pin Descriptions

Pin Number						Name	Function
IMP705/706		IMP707/708		IMP813L			
DIP/SO	MicroSO	DIP/SO	MicroSO	DIP/SO	MicroSO		
1	3	1	3	1	3	$\overline{MR}$	Manual RESET input. The active LOW input triggers a reset pulse. A 250µA pull-up current allows the pin to be driven by TTL / CMOS logic or shorted to ground with a switch.
2	4	2	4	2	4	V_{CC}	+5V power supply input.
3	5	3	5	3	5	GND	Ground reference for all signals.
4	6	4	6	4	6	PFI	Power-fail voltage monitor input. With PFI less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to ground or V_{CC} when not used.
5	7	5	7	5	7	$\overline{PFO}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V.
6	8	—	—	6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6sec at WDI allows the internal timer to run-out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high-impedance three-state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge.
—	—	6	—	—	—	NC	Not connected.
7	1	7	1	—	—	$\overline{RESET}$	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (IMP705: 4.65V, IMP705J: 4.00V, IMP706: 4.40V). $\overline{RESET}$ remains LOW for 200ms after V_{CC} rises above the RESET threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	—	—	8	2	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ pulls LOW when the 1.6 sec internal watchdog timer times-out and does not go HIGH until the watchdog is cleared. In addition, when V_{CC} is below the reset threshold, $\overline{WDO}$ remains low. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as V_{CC} exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
—	—	8	2	7	1	RESET	Active-HIGH reset output. RESET is the inverse of $\overline{RESET}$. The IMP813L has only a RESET output.

Feature Summary

	IMP705	IMP706	IMP707	IMP708	IMP813L
Power-fail detector	■	■	■	■	■
Brownout detection	■	■	■	■	■
Manual RESET input	■	■	■	■	■
Power-up/down RESET	■	■	■	■	■
Watchdog timer	■	■			■
Active-HIGH RESET output			■	■	■
Active-LOW RESET output	■	■	■	■	
RESET threshold	4.65V/4.00V	4.40V	4.65V	4.40V	4.65V

Detail Descriptions

RESET/$\overline{\text{RESET}}$ Operation

The RESET/$\overline{\text{RESET}}$ signals are designed to start a µP/µC in a known state or return the system to a known state.

The IMP707/708 have two RESET outputs, one active-HIGH RESET and one active-LOW RESET output. The IMP813L has only an active-HIGH output. RESET is simply the complement of $\overline{\text{RESET}}$.

$\overline{\text{RESET}}$ is guaranteed to be LOW with V_{CC} above 1.2V. During a power-up sequence, $\overline{\text{RESET}}$ remains low until the supply rises above the threshold level, either 4.65V, 4.40V or 4.00V. $\overline{\text{RESET}}$ goes high approximately 200ms after crossing the threshold.

During power-down, $\overline{\text{RESET}}$ goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4V with V_{CC} above 1.2V.

In a brownout situation where V_{CC} falls below the threshold level, $\overline{\text{RESET}}$ pulses low. If a brownout occurs during an already-initiated reset, the pulse will continue for a minimum of 140ms.

Auxiliary Comparator

All devices have an auxiliary comparator with 1.25V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by a 250µA pull-up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces $\overline{\text{RESET}}$ to be generated. The IMP813L should be used when an active-HIGH RESET is required.

Watchdog Timer

The watchdog timer available on the IMP705/706/813L monitors µP/µC activity. If activity is not detected within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{\text{WDO}}$ will also become LOW and remain so, whenever the supply voltage, V_{CC} , falls below the device threshold level. $\overline{\text{WDO}}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for $\overline{\text{WDO}}$ as there is for the RESET outputs. If WDI is floated, $\overline{\text{WDO}}$ essentially acts as a low-power output indicator.

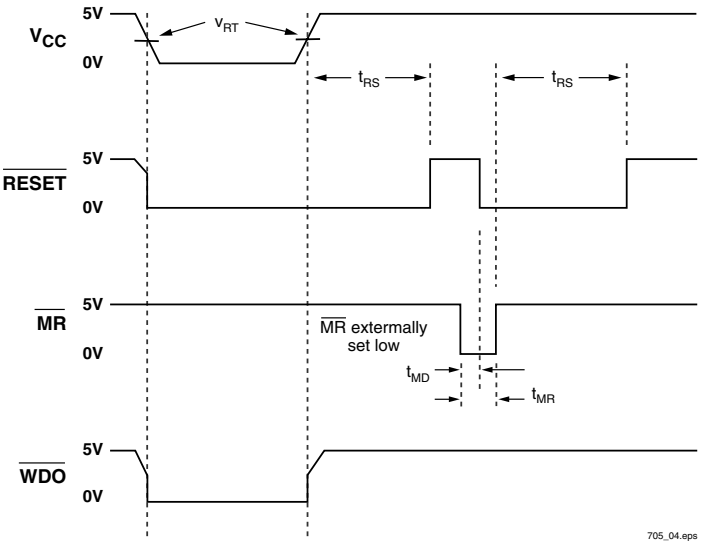


Figure 1. WDI Three-state operation

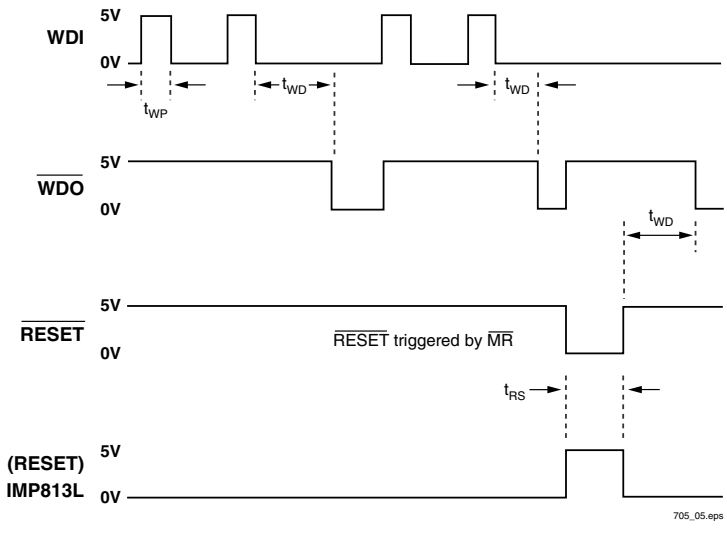


Figure 2. Watchdog Timing

Application Information

Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.1V, the IMP705-708 $\overline{\text{RESET}}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{\text{RESET}}$ to the wrong state, a pull-down resistor should be connected to the $\overline{\text{RESET}}$ pin, thus draining such charges to ground and holding RESET low. The resistor value is not critical. A 100kΩ resistor will pull $\overline{\text{RESET}}$ to ground without loading it.

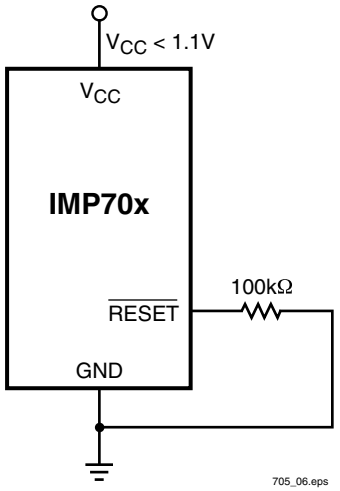


Figure 3. Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0V

Bi-directional Reset Pin Interfacing

The IMP705/6/7/8 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the $\overline{\text{RESET}}$ output and the µP/µC bi-directional $\overline{\text{RESET}}$ pin.

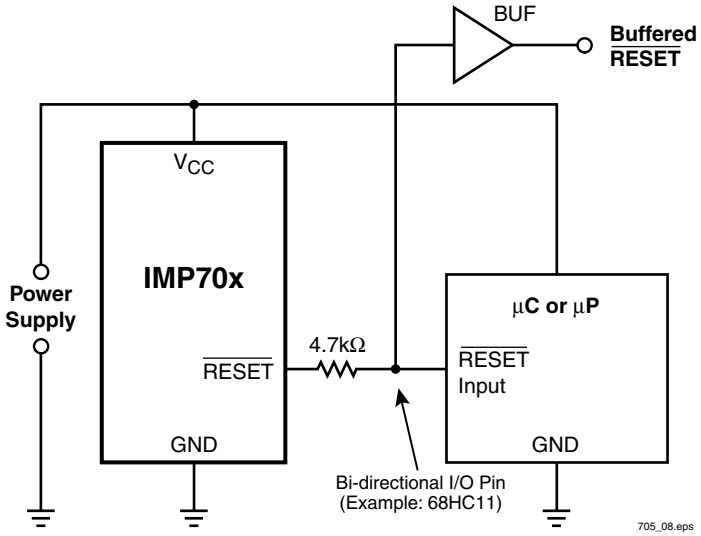


Figure 3. Bi-directional Reset Pin Interfacing

Application Information

Monitoring Voltages Other Than V_{CC}

The IMP705-708 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input, PFI, the $\overline{PFO}$ (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{PFO}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high-frequency noise. If it is desired to assert a RESET in addition to the $\overline{PFO}$ flag, this may be achieved by connecting the $\overline{PFO}$ output to $\overline{MR}$.

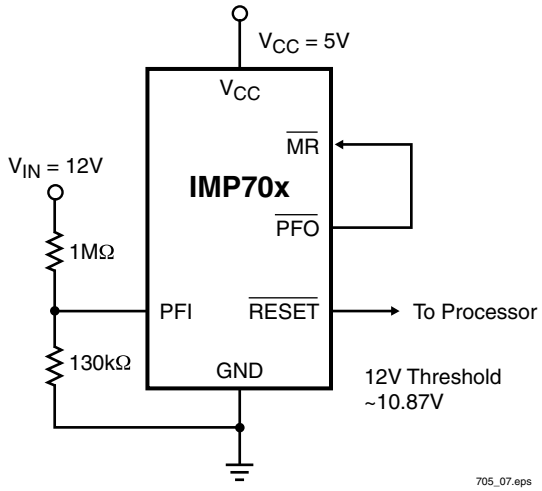


Figure 4. Monitoring Voltages Other Than V_{CC}

Monitoring a Negative Voltage

The Power-Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{PFO}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{PFO}$ goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{RESET}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

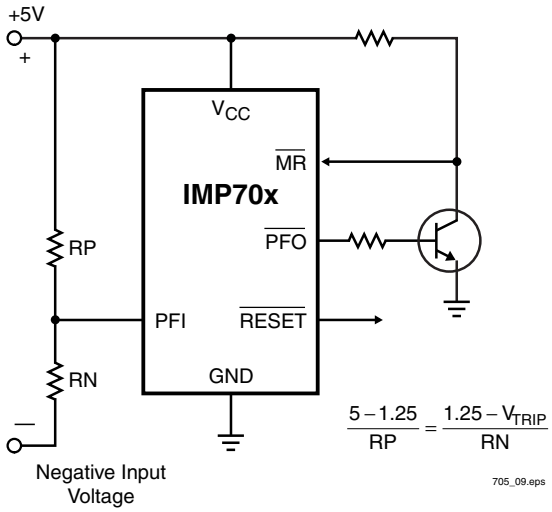
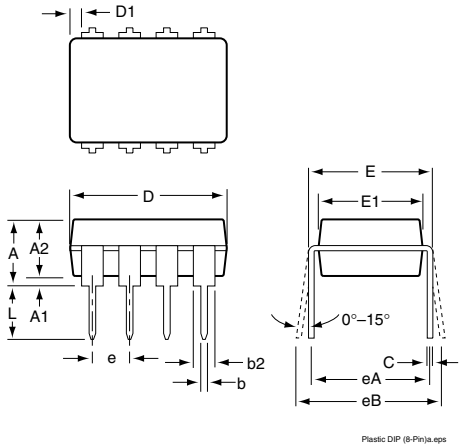


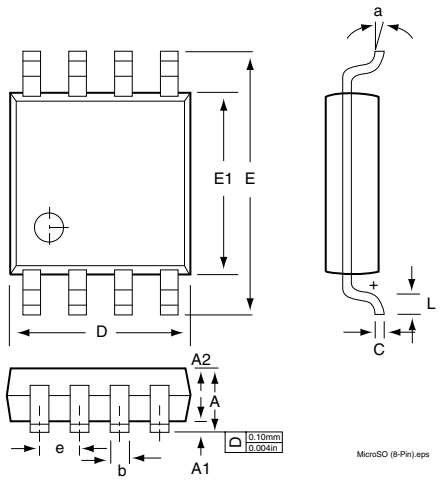
Figure 5. Monitoring a Negative Voltage

Package Dimensions

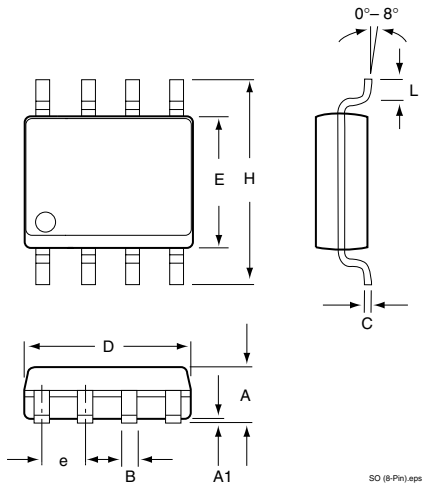
Plastic DIP (8-Pin)*



MicroSO (8-Pin)**



SO (8-Pin)***



	Inches		Millimeters	
	Min	Max	Min	Max
Plastic DIP (8-Pin)				
A	———	0.210	———	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81
MicroSO (8-Pin)				
A	———	0.0433	———	1.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°
SO (8-Pin)				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00

** JEDEC Drawing MS-001BA*
*** JEDEC Drawing MO-187AA*
**** JEDEC Drawing MS-012AA*

ISO 9001 Registered

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