ISO 9001 Registered

Process C1015
CMOS 1.0μm
Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.65	0.85	1.05	V	25 x 1.0μm
Body Factor	γ_N	0.72	0.82	0.92	$V^{1/2}$	25 x 1.0μm
Conduction Factor	β_N	40.0	43.5	47.0	$\mu A/V^2$	25 x 25μm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	μm	25 x 1.0μm
Width Encroachment	ΔW_N		0.25		μm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold	$VTF_{P(N)}$	8			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–1.3	–1.1	–0.9	V	25 x 1.0μm
Body Factor	γ_P	0.46	0.56	0.66	$V^{1/2}$	25 x 1.0μm
Conduction Factor	β_P	12.5	14.0	15.5	$\mu A/V^2$	25 x 25μm
Effective Channel Length	$Leff_P$	0.72	0.97	1.22	μm	25 x 1.0μm
Width Encroachment	ΔW_P		0.3		μm	Per side
Punch Through Voltage	$BVDSS_P$	–8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.65	0.80	1.10	KΩ/☐	n-well
N+ Sheet Resistance	ρ_{N+}	27	37	47	Ω/☐	
N+ Junction Depth	x_{jN+}		0.25		μm	
P+ Sheet Resistance	ρ_{P+}	65	85	110	Ω/☐	
P+ Junction Depth	x_{jP+}		0.3		μm	
Gate Oxide Thickness	T_{GOX}	18.7	20.0	21.3	nm	
Field Oxide Thickness	T_{FIELD}		580		nm	
Gate Poly Sheet Res.	ρ_{POLY1}	25	32	39	Ω/☐	
Top Poly Sheet Resistance	ρ_{POLY2}	18	23	28	Ω/☐	
Metal-1 Sheet Resistance	ρ_{M1}		45		mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}		25		mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.73		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.42	0.5	0.57	$fF/\mu m^2$	

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Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	1.6 / 1.6µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	7.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.0µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	0.8µm
Poly Layers	2	Metal-1 Overlap Of Contact	0.8µm
Contact Size	1.2x1.2µm	Metal-1 Overlap Of Via	0.8µm
Via Size	1.2x1.2µm	Metal-2 Overlap Of Via	0.8µm
Metal-1 Width/Space	1.4 / 1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1015 Process: CMOS 1.0 µm analog technology with 2 levels of metal and Poly-to-Poly capacitors for analog applications.