

Process C1026

BiCMOS 1.0 μ m

Schottky Diode and Low TC P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT _N	0.50	0.70	0.90	V	
Punch Through Voltage	HVBVDSS _N	25			V	
ON Resistance	HVPR _{ON}	200	240	350	Ω	V _{DS} = 0.1V V _{GS} = 5.0V 100x3.0 μ m
Operating Voltage				V _{GS} = 5V V _{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT _N	0.65	0.85	1.05	V	100x1.0 μ m
Body Factor	γ _N	0.75	0.82	0.95	V ^{1/2}	100x1.0 μ m
Conduction Factor	β _N	79.0	87.0	95.0	μ A/V ²	100x100 μ m
Effective Channel Length	Leff _N	0.70	0.90	1.10	μ m	100x1.0 μ m
Width Encroachment	Δ W _N		0.60		μ m	Per side
Punch Through Voltage	BVDSS _N	8	13		V	
Poly Field Threshold Voltage	VTFP _N	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT _P	-0.8	-1.0	-1.2	V	
Punch Through Voltage	HVBVDSS _P	-25			V	
ON Resistance	HVPR _{ON}	400	450	600	Ω	V _{DS} = 0.1V V _{GS} = 5.0V 100x3.5 μ m
Operating Voltage				V _{GS} = -5V V _{DS} = -20V	V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT _P	-1.25	-1.0	-0.85	V	100x1.0 μ m
Body Factor	γ _P	0.40	0.50	0.60	V ^{1/2}	100x1.0 μ m
Conduction Factor	β _P	24.0	28.0	32.0	μ A/V ²	100x100 μ m
Effective Channel Length	Leff _P	0.72	0.97	1.12	μ m	100x1.0 μ m
Width Encroachment	Δ W _P		0.60		μ m	Per side
Punch Through Voltage	BVDSS _P	-8	-12		V	
Poly Field Threshold Voltage	VTF _{P(P)}	-14	-18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C _{OX}		1.727		fF/ μ m ²	
Metal-1 to Poly1	C _{M1P}		0.046		fF/ μ m ²	
Metal-2 to Metal-1	C _{MM}		0.038		fF/ μ m ²	

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Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_t		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		

Schottky Diode	Symbol	Minimum	Typical	Maximum	Unit	Comments
Reverse Bias Breakdown Voltage		-18	-20		V	10x10 μ m
Forward Bias Voltage		0.10	0.15	0.20	V	
ON Resistance			175		Ω	10x10 μ m

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Resistivity		180	230	290	Ω/\square	
TCR		-100	0	+50	ppm/ $^{\circ}$ C	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω -cm	
Well (field) Sheet Resistance	$\rho_{N-well(f)}$	0.65	0.80	1.10	$K\Omega/\square$	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/\square	
N+ Junction Depth	x_{jN+}		0.45		μ m	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/\square	
P+ Junction Depth	x_{jP+}		0.50		μ m	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	IP_{OX}		47			
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	$m\Omega/\square$	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0 μ m	Contact to Poly Space	1.0 μ m
Min spacing, active region, 5V	1.2 μ m	Contact Overlap of Diffusion	1.0 μ m
Min spacing, active region, 12V	2.0 μ m		
Poly1 (Gate) Width/Space	1.0/1.4 μ m	Contact Overlap of Poly	0.8 μ m
Poly2 Width/Space	1.6/2.0 μ m	Metal-1 Overlap of Contact	0.8 μ m
Contact Width/Space	1.2x1.2 μ m	Metal-1 Overlap of Via	0.8 μ m
Metal-1 Width/Space	1.4/1.2 μ m	Minimum Pad Opening	65x65 μ m
Metal-2 Width/Space	1.8/1.4 μ m	Minimum Pad to Pad Spacing	5.0 μ m
Via Width/Space	1.2/1.8 μ m	Minimum Pad Pitch	80 μ m