ISO 9001 Registered

Process C1027
BiCMOS 1.0μm
Low TC P-Poly Resistor

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.50	0.70	0.90	V	
Punch Through Voltage	$HVBVDSS_N$	25			V	
ON Resistance	$HVPR_{0N}$	200	240	350	Ω	100x2.0μm
Operating Voltage				V_{GS} = 5V V_{DS} = 20V	V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.65	0.85	1.05	V	100x1.0μm
Body Factor	γ_N	0.75	0.85	0.95	$V^{1/2}$	100x1.0μm
Conduction Factor	β_N	79.0	87.0	95.0	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	0.70	0.90	1.10	μm	100x1.0μm
Width Encroachment	ΔW_N		0.60		μm	Per side
Punch Through Voltage	$BVDSS_N$	8	13		V	
Poly Field Threshold Voltage	$VTFP_N$	14	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	–1.25	–1.05	–0.85	V	100x1.0μm
Body Factor	γ_P	0.4	0.5	0.6	$V^{1/2}$	100x1.0μm
Conduction Factor	β_P	24.0	28.0	32.0	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	0.72	0.97	1.12	μm	100x1.0μm
Width Encroachment	ΔW_P		0.60		μm	Per side
Punch Through Voltage	$BVDSS_P$	–8	–12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–14	–18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		1.727		$fF/\mu m^2$	
Metal-1 to Poly1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.038		$fF/\mu m^2$	

Electrical Characteristics

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	100	150		4.5x4.5mm
Early Voltage	V_{AN}	30	34			
Cut-Off Frequency	f_{τ}		6.2		GHz	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	10	40	100		
Early Voltage	V_{AP}		TBD		V	

Low TCR P-Poly Resistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Resistivity		180	230	290	Ω/☐	
TCR		–100	0	+50	ppm/˚C	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>		25		50	Ω-cm	
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.65	0.80	1.10	KΩ/☐	n-well
N+ Sheet Resistance	ρ_{N+}	22.0	37.0	50.0	Ω/☐	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	40.0	57.0	80.0	Ω/☐	
P+ Junction Depth	x_{jP+}		0.50		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		20		nm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Interpoly Oxide Thickness	$I\rho_{OX}$		47		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	23.0	38.0	53.0	Ω/☐	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

Min Channel Width	2.0µm	Contact to Poly Space	1.0µm
Min spacing, active region, 5V	1.2µm	Contact Overlap of Diffusion	1.0µm
Min spacing, active region, 12V	2.0µm		
Poly1 (Gate) Width/Space	1.0/1.4µm	Contact Overlap of Poly	0.8µm
Poly2 Width/Space	1.6/2.0µm	Metal-1 Overlap of Contact	0.8µm
Contact Width/Space	1.2x1.2µm	Metal-1 Overlap of Via	0.8µm
Metal-1 Width/Space	1.4/1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	1.8/1.4µm	Minimum Pad to Pad Spacing	5.0µm
Via Width/Space	1.2/1.8µm	Minimum Pad Pitch	80µm