

Process C1201

CMOS 1.2 μ m

Digital Double-Metal

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_N}	0.55	0.75	0.95	V	100x1.2 μ m
Body Factor	γ_N		0.34		V ^{1/2}	100x1.2 μ m
Conduction Factor	β_N	64	75	86	μ A/V ²	100x100 μ m
Effective Channel Length	L_{effN}	0.8	1.0	1.2	μ m	100x1.2 μ m
Width Encroachment	ΔW_N		0.6		μ m	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_P}	-0.7	-0.9	-1.1	V	100x1.2 μ m
Body Factor	γ_P		0.38		V ^{1/2}	100x1.2 μ m
Conduction Factor	β_P	21	25	29	μ A/V ²	100x100 μ m
Effective Channel Length	L_{effP}	0.9	1.1	1.3	μ m	100x1.2 μ m
Width Encroachment	ΔW_P		0.8		μ m	Per side
Punch Through Voltage	$BVDSS_P$	-9			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-10			V	

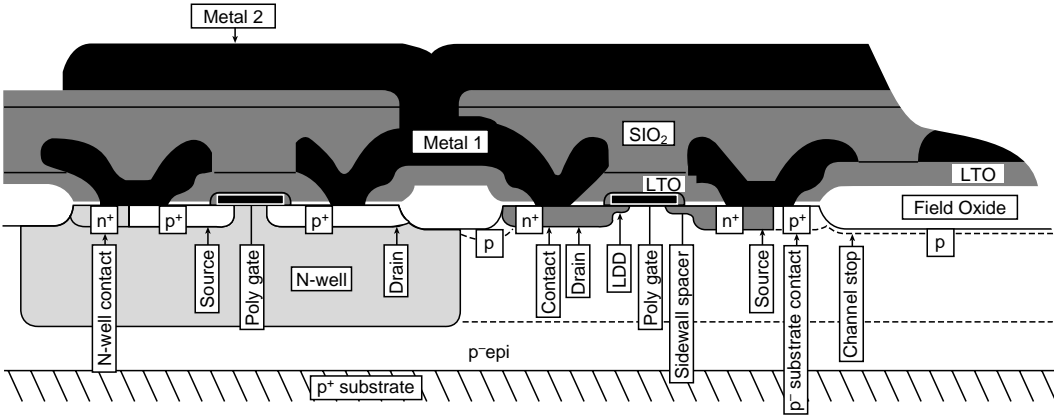
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N-well(f)}$	0.6	1.0	1.3	K Ω/\square	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/\square	
N+ Junction Depth	x_{jN+}		0.35		μ m	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/\square	
P+ Junction Depth	x_{jP+}		0.35		μ m	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Res.	ρ_{POLY1}	15	22	30	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}		50		m Ω/\square	
Metal-2 Sheet Resistance	ρ_{M2}		30		m Ω/\square	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/ μ m ²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/ μ m ²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/ μ m ²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/ μ m ²	

Physical Characteristics

Starting Material	EPI P <100>	N+/P+ Width/Space	2.0 / 1.2μm
Starting Mat. Resistivity	7 - 8.5 Ω-cm	N+ To P+ Space	9.0μm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5μm
Well Type	N-well	Contact Overlap Of Diffusion	1.0μm
Metal Layers	2	Contact Overlap Of Poly	1.0μm
Poly Layers	1	Metal-1 Overlap Of Contact	1.0μm
Contact Size	1.5x1.5μm	Metal-1 Overlap Of Via	1.0μm
Via Size	1.5x1.5μm	Metal-2 Overlap Of Via	1.0μm
Metal-1 Width/Space	2.5 / 1.5μm	Minimum Pad Opening	65x65μm
Metal-2 Width/Space	2.5 / 1.5μm	Minimum Pad-to-Pad Spacing	5.0μm
Gate Poly Width/Space	1.5 / 2.0μm	Minimum Pad Pitch	80.0μm

Special Feature of C1201 Process: CMOS 1.2 μm digital technology with 1 poly and 2 levels of metal.



Cross-sectional view of the MxCMOS 1.2 process

