Process C1215
CMOS 1.2μm
Low Threshold Devices

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.3	0.475	0.65	V	100x1.2μm
Body Factor	γ_N	0.29	0.36	0.44	$V^{1/2}$	100x1.2μm
Conduction Factor	β_N	75	90	105	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	0.8	1.0	1.2	μm	100x1.2μm
Width Encroachment	ΔW_N		0.6		μm	Per side
Punch Through Voltage	$BVDSS_N$	9			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	10			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.3	–0.475	–0.65	V	100x1.2μm
Body Factor	γ_P	0.4	0.5	0.7	$V^{1/2}$	100x1.2μm
Conduction Factor	β_P	18	23	28	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	0.9	1.1	1.3	μm	100x1.2μm
Width Encroachment	ΔW_P		0.8		μm	Per side
Punch Through Voltage	$BVDSS_P$	–9.0			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10.0			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.8	1.4	2.0	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		μm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		μm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Field Oxide Thickness	T_{FIELD}		800		nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Top Poly Sheet Reistance	ρ_{POLY2}		35		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.035		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+ To P+ Space	9.0µm
Max Operating Voltage	3V-5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

Special Feature of C1215 Process: Low threshold n- and p-channel transistors in CMOS 1.2 µm technology.