ISO 9001 Registered

Process C1216

CMOS 1.2µm

15 Volt Operation

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.75	0.95	1.15	V	100x1.5µm
Body Factor	γ_N		0.81		$V^{1/2}$	100x1.5µm
Conduction Factor	β_N	37	46	55	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_N$		1.35	2	µm	100x1.5µm
Width Encroachment	ΔW_N		0.665		µm	Per side
Punch Through Voltage	$BVDSS_N$	18	21		V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	18	20		V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.80	–1.00	–1.20	V	100x1.2µm
Body Factor	γ_P		0.65		$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	11	15	20	$\mu A/V^2$	100x100µm
Effective Channel Length	$Leff_P$		1.5		µm	100x1.2µm
Width Encroachment	ΔW_P		0.7		µm	Per side
Punch Through Voltage	$BVDSS_P$	–18	–21		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–18	–20		V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.4	1.8	2.2	KΩ/☐	n-well
N-well Junction Depth	X_{JNWELL}		3.0		µm	
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/☐	
N+ Junction Depth	x_{jN+}		0.6		µm	
P+ Sheet Resistance	ρ_{P+}	50	75	100	Ω/☐	
P+ Junction Depth	x_{jP+}		0.4		µm	
Gate Oxide Thickness (HV)	T_{GOX}		48		nm	
Field Oxide Thickness	T_{FIELD}		1000		nm	
Gate Poly Sheet Resistance	ρ_{POLY2}	15	22	30	Ω/☐	
Bottom Poly Sheet Res.	ρ_{POLY1}	20	25	30	Ω/☐	
Metal-1 Sheet Resistance	ρ_{M1}		42		mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}	19	25	32	mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		0.719		$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}		0.028		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}		0.050		$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.69	0.86	1.03	$fF/\mu m^2$	

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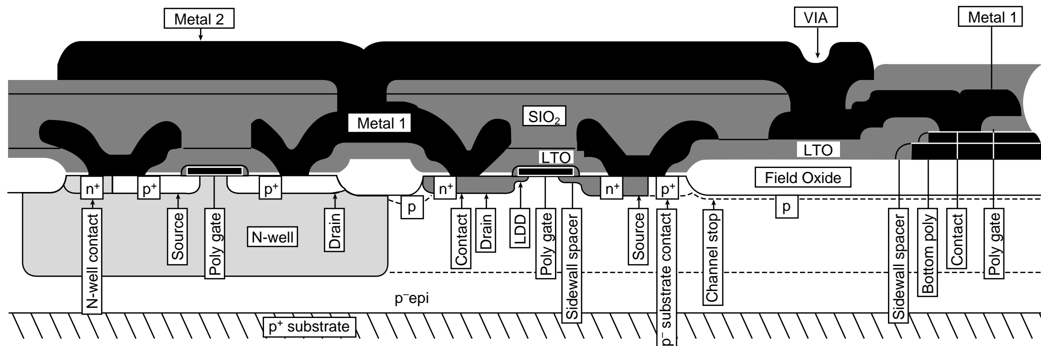
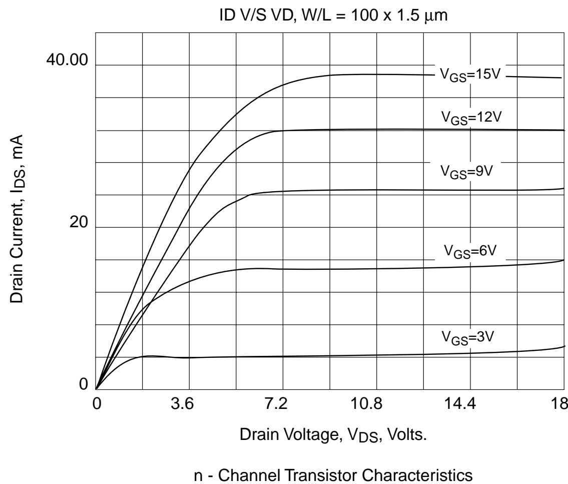
Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.5 / 2.0µm
Starting Mat. Resistivity	4 - 6.6 Ω-cm	N+ To P+ Space	9.0µm
Operating Voltage	15V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	1.0µm
Metal Layers	2	Contact Overlap Of Poly	1.0µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad Pitch	80.0µm

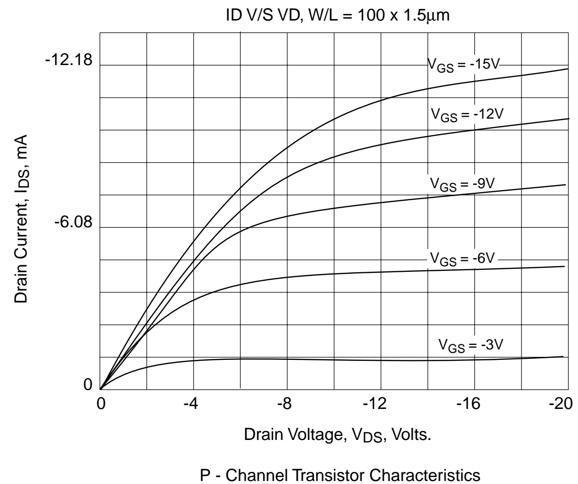
Special Feature of C1216 Process: 15 Volt operating n- and p-channel transistors are available along with 5 Volt CMOS 1.2 µm devices.



Similar structures with offset source/drain for 15V devices



n - Channel Transistor Characteristics



P - Channel Transistor Characteristics