Process C1226
CMOS 1.2µm
100V CMOS, Double Metal - Double Poly

Electrical Characteristics

T = 25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.70	0.90	1.10	V	
Punch Through Voltage	$HVBVDSS_N$	120			V	
ON Resistance	$HVPR_{0N}$	550	700	850	Ω	W/L = 147/5
Operating Voltage			V_{GS} = 5V V_{DS} = 100V			
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.30	0.45	0.65	V	100x1.5µm
Body Factor	γ_N		0.475		$V^{1/2}$	100x1.5µm
Conduction Factor	β_N	64	78	92	µA/V²	100x100µm
Effective Channel Length	$Leff_N$		1.35		µm	100x1.5µm
Width Encroachment	ΔW_N		0.4		µm	Per side
Punch Through Voltage	$BVDSS_N$	5	12		V	
Poly Field Threshold Voltage	$VTFP_N$	8	15		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	−0.70	−0.90	−1.10	V	
Punch Through Voltage	$HVBVDSS_P$	−120			V	
ON Resistance	$HVPR_{0N}$	2000	2500	3000	Ω	W/L = 139/5
Operating Voltage			V_{GS} = 5V V_{DS} = 100V		V	
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	-0.65	−0.45	−0.30	V	100x1.5µm
Body Factor	γ_P		0.6		$V^{1/2}$	100x1.5µm
Conduction Factor	β_P	20	25	30	µA/V²	100x100µm
Effective Channel Length	$Leff_P$		1.5		µm	100x1.5µm
Width Encroachment	ΔW_P		0.4		µm	Per side
Punch Through Voltage	$BVDSS_P$	−5	−12		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−8	−12		V	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well (field) Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.0	1.7	2.4	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.3		µm	
P+ Sheet Resistance	ρ_{P+}	60	110	150	Ω/□	
P+ Junction Depth	x_{jP+}		0.3		µm	
High-Voltage Gate Oxide Th	HT_{GOX}		24		nm	
Gate Oxide Thickness	T_{GOX}		24		nm	
Interpoly Oxide	IP_{OX}	33.6	42.0	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}		30.0		Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		45		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		29		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Layout Rules

High Voltage Section Rules

Min Channel Width	4.0µm	Diffusion Overlap of Contact	1.0µm
Min Spacing, Active Region, 5V	2.0µm	Poly Overlap of Contact	1.0µm
Poly1 Width/Space	1.5/2.0µm	Contact to Poly Space	1.5µm
Poly2 Width/Space	3.0/2.0µm	Metal-1 Overlap of Contact	1.0µm
Contact Width/Space	1.5/1.5µm	Minimum Pad Opening	65x65µm
Via Width/Space	1.5/1.5µm	Minimum Pad to Pad Spacing	5.0µm
Metal-1 Width/Space	2.5/1.5µm	Minimum Pad Pitch	80µm
Metal-2 Width/Space	2.5/1.5µm		