Process C1227
HV BiCMOS 1.2μm
30V Double Metal - Double Poly

Electrical Characteristics

T=25°C Unless otherwise noted

	Symbol	Minimum	Typical	Maximum	Unit	Comments
N-Channel High Voltage Transistor						
Threshold Voltage	HVT_N	0.7	0.9	1.1	V	
Punch Through Voltage	$HVBVDSS_P$	36			V	
ON Resistance	$HVPR_{0N}$		1.4		mΩ-cm²	@V_{GS} = 5V V_{DS} = 0.1V
Operating Voltage			V_{GS} = 5V V_{DS} = 30V		V	
N-Channel Low Voltage Transistor						
Threshold Voltage	VT_N	0.4	0.6	0.8	V	100x1.4μm
Body Factor	γ_N	0.50	0.65	0.80	$V^{1/2}$	100x1.4μm
Conduction Factor	β_N	64.0	75.0	86.0	μA/V²	100x100μm
Effective Channel Length	$Leff_N$	1.20	1.35	1.50	μm	100x1.4μm
Width Encroachment	ΔW_N		0.45		μm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTFP_N$	10	18		V	

	Symbol	Minimum	Typical	Maximum	Unit	Comments
P-Channel High Voltage Transistor						
Threshold Voltage	HVT_P	−0.7	−0.9	−1.1	V	
Punch Through Voltage	$HVBVDSS_P$	−36			V	
ON Resistance	$HVPR_{0N}$		11.0		mΩ-cm²	@V_{GS} = −5V @V_{DS} = −0.1V
P-Channel Low Voltage Transistor						
Threshold Voltage	VT_P	−0.8	−0.6	−0.4	V	100x1.4μm
Body Factor	γ_P	0.35	0.50	0.65	$V^{1/2}$	100x1.4μm
Conduction Factor	β_P	20.0	25.0	30.0	μA/V²	100x100μm
Effective Channel Length	$Leff_P$	1.35	1.50	1.65	μm	100x1.4μm
Width Encroachment	ΔW_P		0.40		μm	Per side
Punch Through Voltage	$BVDSS_P$	−8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−10	−18		V	

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.338	1.439	1.569	fF/μm²	
Metal-1 to Poly1	C_{M1P}	0.040	0.046	0.052	fF/μm²	
Metal-2 to Metal-1	C_{MM}	0.043	0.050	0.057	fF/μm²	

Vertical NPN Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	h_{FE}	50	140	240		4.5x4.5μm
Early Voltage	V_A		34		V	
Cut-Off Frequency	f_τ		1.89		GHz	

Physical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Starting Material p<100>						
Well(field)Sheet Resistance	$\rho_{N\text{-}well(f)}$	1.5	2.1	2.7	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20.0	35.0	50.0	Ω/□	
N+ Junction Depth	x_{jN+}		0.4		µm	
P+ Sheet Resistance	ρ_{P+}	50.0	75.0	100.0	Ω/□	
P+ Junction Depth	x_{jP+}		0.4		µm	
Base Resistance	RSHB_RB	1.33	1.66	2.00	KΩ/sq	
High-Voltage Gate Oxide	HT_{GOX}		22		nm	
Gate Oxide Thickness	T_{GOX}		22		nm	
Interpoly Oxide Thickness	IP_{OX}	33.6	42	50.4	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15.0	22.0	30.0	Ω/□	
Poly2 Resistivity	RSH_PL P	1.5	2	2.5	kΩ/□	
Metal-1 Sheet Resistance	ρ_{M1}	35.0	45.0	65.0	mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}	19.0	25.0	35.0	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nitride

Layout Rules

Min Channel Width	4.0µm	Diffusion Overlap of Contact	1.0µm
Min Spacing, Active Region, 5V	2.0µm	Poly Overlap of Contact	1.0µm
Poly1 Width/Space	1.4/2.0µm	Metal-1 Overlap of Contact	1.5µm
Poly2 Width/Space	3.0/2.0µm	Contact to Poly Space	1.5µm
Contact Width/Space	1.4x1.4µm	Minimum Pad Opening	65x65µm
Via Width/Space	1.4/1.6µm	Metal-1 Overlap of Via	1.0µm
Metal-1 Width/Space	2.6/1.6µm	Metal-2 Overlap of Via	1.0µm
Metal-2 Width/Space	2.6/1.6µm	Minimum Pad Opening	65x65µm
Gate Poly Width/Space	1.5/2.0µm	Minimum Pad to Pad Spacing	5.0µm
N+/P+ Width/Space	2.5/2.0µm	Minimum Pad Pitch	80µm