ISO 9001 Registered

Process C1232

CMOS 1.2µm EEPROM with Lateral PNP

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.30	0.475	0.65	V	100x10µm
Body Factor	γ_N	0.35	0.45	0.55	$V^{1/2}$	100x100µm
Conduction Factor	β_N	64	78	92	µA/V^2	100x100µm
Saturation Current	I_{DSATN}	16	25	40	mA	100x1.5µm
Punch Through Voltage	$BVDSS_N$	5			V	
Poly Field Threshold	$VTF_{P(N)}$	8			V	

N-Channel Native Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_{ZBN}	−0.20	0.37	0.52	V	100x2.5µm
Body Factor	γ_{ZBN}	0.30	0.45	0.60	$V^{1/2}$	100x2.5µm
Saturation Current	I_{DSATN}	13	15.7	18.9	mA	100x2.5µm
Conduction Factor	β_{ZBN}	45	55	65	µA/V^2	100x100µm

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	−0.65	−0.475	0.30	V	100x1.2µm
Body Factor	γ_P	0.5	0.6	0.7	$V^{1/2}$	100x1.2µm
Conduction Factor	β_P	20	25	30	µA/V^2	100x100µm
Saturation Current	I_{DSATP}	−6	−10	−16	mA	100x1.5µm
Punch Through Voltage	$BVDSS_P$	−5			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	−8			V	

EECMOS Characteristics	Symbol	Minimum	Typical	Maximum	Unit	Comments
Tunnel Oxide Thickness	T_{TUNLOX}	84	88	92	nm	
Interpoly Oxide Thickness	T_{P1P2}	340	390	440	nm	
Buried N+ Sheet Res.	ρ_{BN+}	200	300	400	Ω/□	
Initial Program/Erase Window			3.0		V	
Unprog. Memory Threshold	V_T		3.0		V	
Endurance		10,000			Cycles	
Programming Voltage	VPP	12	14	17	V	

Lateral PNP	Symbol	Minimum	Typical	Maximum	Unit	Comments
Beta	H_{FE}	10	35	100		
Early Voltage	V_{AP}		TBD		V	

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Electrical Characteristics

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.2	20	2.8	KΩ/☐	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/☐	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	60	110	160	Ω/☐	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}	22.5	25.0	27.5	nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Gate Poly Sheet Res.	ρ_{POLY2}	25	35	45	Ω/☐	
Bottom Poly Sheet Res.	ρ_{POLY1}	24	32	40	Ω/☐	
High Resistance Poly	ρ_{POLYHI}	1.5	2.0	2.5	kΩ/☐	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/☐	
Metal-2 Sheet Resistance	ρ_{M2}	19	25	32	mΩ/☐	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.28	1.38	1.58	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.057		fF/µm²	
Metal-1 to Silicon	C_{M1S}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.035		fF/µm²	
Poly-1 to Poly-2	C_{P1P1}		0.86		fF/µm²	

Physical Characteristics

Starting Material	P <100>	High Poly Width/Space	1.5 / 1.5µm
Starting Mat. Resistivity	25 - 50 Ω-cm	N+/P+ Width/Space	2.0 / 2.0µm
Epi Layer	P Type, 7 - 8.5 Ω-cm with N+ Buried Layer	N+ To P+ Space	9.0µm
		Tunnel Oxide Width/Space	1.5 / 1.5µm
Operating Voltage	5V	Tunnel Ox. Overlap Bot. Poly	1.0µm
Well Type	N-well	Contact To Poly Space	1.5µm
Metal Layers	2	Contact Overlap Of Diffusion	1.0µm
Poly Layers	2	Contact Overlap Of Poly	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Contact	1.0µm
Via Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Metal-1 Width/Space	2.5 / 1.5µm	Metal-2 Overlap Of Via	1.0µm
Metal-2 Width/Space	2.5 / 1.5µm	Minimum Pad Opening	65x65µm
Gate Poly Width/Space	1.5 / 2.0µm	Minimum Pad-to-Pad Spacing	5.0µm
Buried N+ Width/Space	2.5 / 1.75µm	Minimum Pad Pitch	80.0µm

Special Feature of C1232 Process: EEPROM process with high resistivity poly resistors and native n-channel devices.