Process C1601
CMOS 1.6µm
Analog Mixed Mode

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.47	0.67	0.87	V	25x1.6µm
Body Factor	γ_N	0.6	0.75	0.90	$V^{1/2}$	25x1.6 µm
Conduction Factor	β_N	33	39	45	$\mu A/V^2$	25x25µm
Effective Channel Length	$Leff_N$	1.0	1.3	1.6	µm	25x1.6 µm
Width Encroachment	ΔW_N		0.0		µm	Per side
Punch Through Voltage	$BVDSS_N$	8			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	8			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–1.1	–0.9	–0.7	V	25x1.6 µm
Body Factor	γ_P	0.27	0.42	0.57	$V^{1/2}$	25x1.6 µm
Conduction Factor	β_P	10.0	12.5	15.0	$\mu A/V^2$	25x25µm
Effective Channel Length	$Leff_P$	1.12	1.42	1.72	µm	25x1.6 µm
Width Encroachment	ΔW_P		0.0		µm	Per side
Punch Through Voltage	$BVDSS_P$	–8			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–8			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	1.6	2.0	2.4	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	25	35	45	Ω/□	
N+ Junction Depth	x_{jN+}		0.35		µm	
P+ Sheet Resistance	ρ_{P+}	74	94	114	Ω/□	
P+ Junction Depth	x_{jP+}		0.35		µm	
Gate Oxide Thickness	T_{GOX}	225	250	275	nm	
Field Oxide Thickness	T_{FIELD}	550	650	750	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Bottom Poly Sheet Res.	ρ_{POLY2}	29	37	45	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	1.23	1.38	1.53	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.046		$fF/\mu m^2$	
Metal-2 to Metal-1	C_{MM}	0.033	0.037	0.041	$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	
Poly-1 to Poly-2	C_{P1P2}	0.43	0.53	0.63	$fF/\mu m^2$	

Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	1.6 / 3.2µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	8.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	1.5µm
Well Type	N-well	Contact Overlap Of Diffusion	0.8µm
Metal Layers	2	Contact Overlap Of Poly	0.8µm
Poly Layers	2	Metal-1 Overlap Of Contact	1.0µm
Contact Size	1.5x1.5µm	Metal-1 Overlap Of Via	1.0µm
Via Size	1.5x1.5µm	Metal-2 Overlap Of Via	1.2µm
Metal-1 Width/Space	2.0 / 2.0µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	3.2 / 2.3µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.6 / 1.7µm	Minimum Pad Pitch	80.0µm

Special Feature of C1601 Process: 2.0 µm Analog process with n- and p-channel transistors in CMOS 1.5 µm technology.