

Process C5014

CMOS 5 μ m

15 Volt Analog

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_N}	0.7	0.9	1.0	V	100x100 μ m
Body Factor	γ_N	1.2	1.4	1.6	$V^{1/2}$	100x100 μ m
Conduction Factor	β_N	23	25.5	30	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{effN}	2.33	2.85	3.33	μ m	100x100 μ m
Width Encroachment	ΔW_N		1.0		μ m	Per side
Punch Through Voltage	$BVDSS_N$	20	25		V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	20			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	V_{T_P}	-0.7	-0.9	-1.1	V	100x100 μ m
Body Factor	γ_P	0.6	0.75	0.9	$V^{1/2}$	100x100 μ m
Conduction Factor	β_P	7.5	9.0	10.5	$\mu A/V^2$	100x100 μ m
Effective Channel Length	L_{effP}	2.92	3.34	3.82	μ m	100x100 μ m
Width Encroachment	ΔW_P		1.5		μ m	Per side
Punch Through Voltage	$BVDSS_P$	-20	-25		V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	-20			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P-well(f)}$	4	5	6	$K\Omega/\square$	P-well
N+ Sheet Resistance	ρ_{N+}	10	13	15	Ω/\square	
N+ Junction Depth	x_{jN+}		1.5		μ m	
P+ Sheet Resistance	ρ_{P+}	30	50	75	Ω/\square	
P+ Junction Depth	x_{jP+}		1.2		μ m	
Gate Oxide Thickness	T_{GOX}	100	108	118	nm	
Interpoly Oxide Thickness	T_{P1P2}	56	66	76	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	12	15	30	Ω/\square	
Top Poly Sheet Res.	ρ_{POLY2}	20	30	40	Ω/\square	
Metal-1 Sheet Resistance	ρ_{M1}		25	60	$m\Omega/\square$	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}		0.321		fF/ μ m ²	
Metal-1 to Poly-1	C_{M1P}		0.036		fF/ μ m ²	
Metal-1 to Silicon	C_{M1S}		0.019		fF/ μ m ²	
Poly-1 to Poly-2	C_{P1P2}	0.436	0.57	0.704	fF/ μ m ²	

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Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 5.0 μ m
Starting Mat. Resistivity	3 - 6 Ω -cm	N+ To P+ Space	5.0 μ m
Typ. Operating Voltage	15V	Contact To Poly Space	3.0 μ m
Well Type	P-well	Contact Overlap Of Active	2.0 μ m
Metal Layers	1	Contact Overlap Of Poly	1.0 μ m
Poly Layers	2	Metal-1 Overlap Of Contact	1.0 μ m
Contact Size	3.0x3.0 μ m	Minimum Pad Opening	100x100 μ m
Metal-1 Width/Space	5.0 / 3.0 μ m	Minimum Pad-to-Pad Spacing	5.0 μ m
Gate Poly Width/Space	5.0 / 2.5 μ m	Minimum Pad Pitch	80.0 μ m

Special Feature of C5014 Process: 15 Volt P-well single metal analog process in CMOS 5.0 μ m technology.